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AN00094

TJA1041/1041A high speed CAN transceiver

Rev. 03 — 8 November 2006

Application note

Document information

Info	Content
Keywords	Controller Area Network (CAN), ISO11898, Transceiver, Physical Layer, TJA1040, TJA1041, TJA1050, PCA82C250/C251
Abstract	<p>The TJA1041/TJA1041A is an advanced high speed CAN transceiver for use in automotive and general industrial applications. CAN (Controller Area Network) has become the de-facto standard protocol for serial in-vehicle bus communication, particularly for Powertrain and Body Multiplexing.</p> <p>The TJA1041/TJA1041A features the low power management known from the Fault Tolerant CAN Transceiver TJA1054. Accordingly, the TJA1041/TJA1041A is predestined for Electronic Control Units (ECUs), which are continuously supplied by battery regardless of ignition key. Furthermore, the TJA1041/TJA1041A offers enhanced diagnosis features. Local failures, like short circuits between pins, as well as bus wiring failures are detected and reported to the host microcontroller.</p> <p>Interoperability with the high speed CAN transceivers PCA82C250/251, TJA1050 and TJA1040 from NXP Semiconductors is also considered.</p>

Revision history

Rev	Date	Description
03.00	20061108	Updated version <ul style="list-style-type: none">• The format of this application note has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Update of Section 6.2 “Application of common mode choke”.• Update of Section 6.3 “ESD protection”.
	20040603	Updated version <ul style="list-style-type: none">• Update of chapter “Target Application for the TJA1041”.• Update of chapter “Hardware Application of the TJA1041”.• Update of chapter “Undervoltage Detection”.• Update of sub-chapter “Vcc Supply Buffering”.• New sub-chapter “Application of common mode choke”.• New sub-chapter “ESD Protection”.• New sub-chapter “PCB layout rules”.• New chapter “Wakeup Detection”.• New chapter “Pin FMEA”.• New sub-chapter “Differences between TJA1041 and TJA1041A”.
02.00	20020925	Updated version <ul style="list-style-type: none">• New chapter “Target Applications for the TJA1041”.• Update of chapter “Hardware Application of the TJA1041”.• New chapter “Flag Signalling”.• Previous chapter “Diagnosis” split into chapter “Bus Failure Diagnosis” and “Local Failure Diagnosis”.• New chapter “Under-voltage Detection”.• Update of chapter “Interoperability”.
01.00	20010419	Initial version

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1. Introduction

The TJA1041/TJA1041A high speed CAN transceiver [Ref. 1](#) from NXP Semiconductors provides the physical link between the protocol controller and the physical transmission medium according to ISO11898 [Ref. 2](#) and SAE J2284 [Ref. 3](#). It has been developed to address mainly those control applications within automotive electronics, which remain supplied by the battery during the whole lifetime of the vehicle. Focusing on these applications the TJA1041/TJA1041A offers a low power management similar to that of the Fault-tolerant CAN Transceiver TJA1054 [Ref. 4](#). According to this concept one or more external voltage regulators within the Electronic Control Unit (ECU) are controlled autonomously by the transceiver. This concept allows a TJA1041/TJA1041A entering Sleep mode to switch these voltage regulators off, disabling the V_{CC} supply of the transceiver and the host microcontroller.

The TJA1041/TJA1041A is available without packaging (bare die) as well as in an SO14 package as shown in [Figure 1](#). The upper part of the SO14 pinning is compatible with the SO8 pinning of other high speed CAN transceivers from NXP Semiconductors, like the PCA82C250 [Ref. 5](#), PCA82C251 [Ref. 6](#), TJA1050 [Ref. 7](#) and TJA1040 [Ref. 8](#).

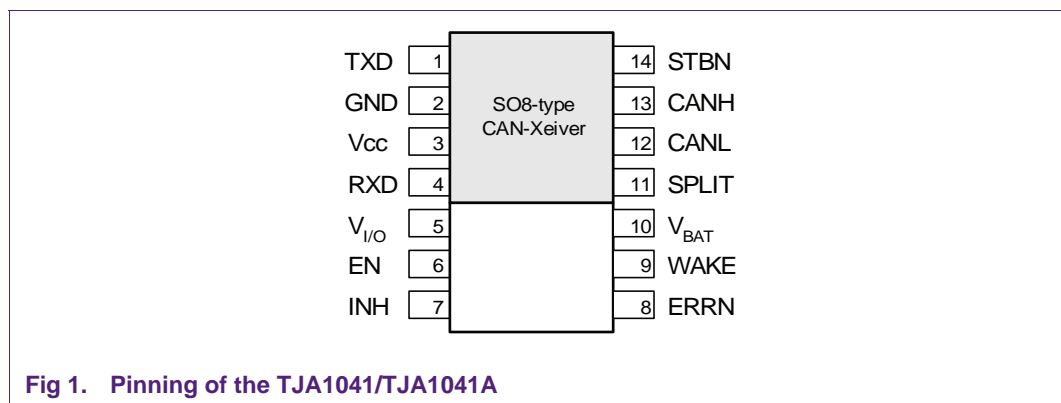


Fig 1. Pinning of the TJA1041/TJA1041A

2. General application of high speed CAN

A general application of high speed CAN is illustrated in [Figure 2](#). Here a linear bus topology is shown with the ECUs connected to the bus via stubs. Both bus ends are terminated with $120\ \Omega$, resulting in the nominal $60\ \Omega$ bus load according to ISO11898 [Ref. 2](#). [Figure 2](#) shows the Split Termination concept, which helps improve the EMC of high speed CAN bus systems [Ref. 9](#). The former single $120\ \Omega$ termination resistor is split into two resistors of half value with the center tap connected to ground via the capacitor C_{spl} .

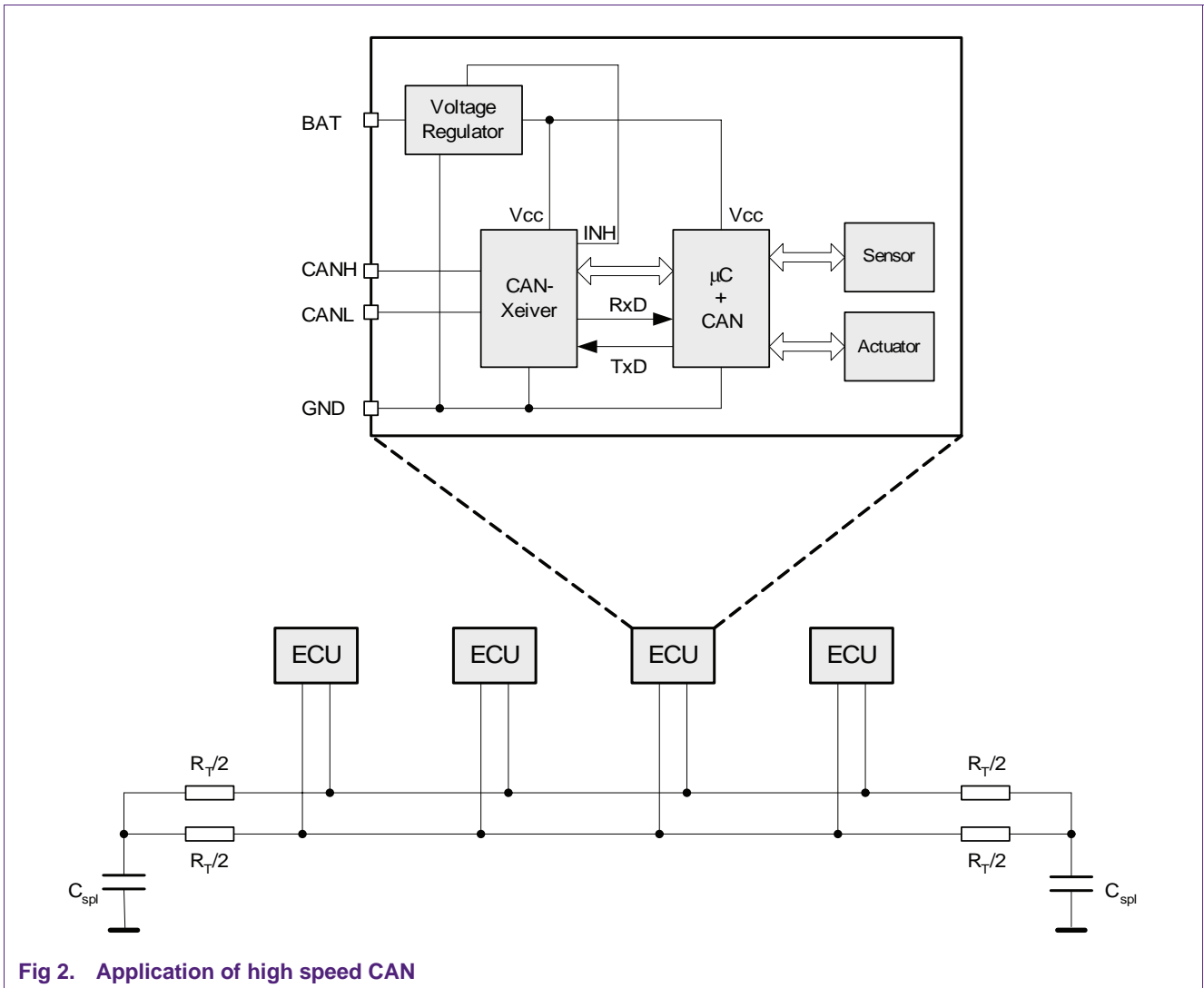


Fig 2. Application of high speed CAN

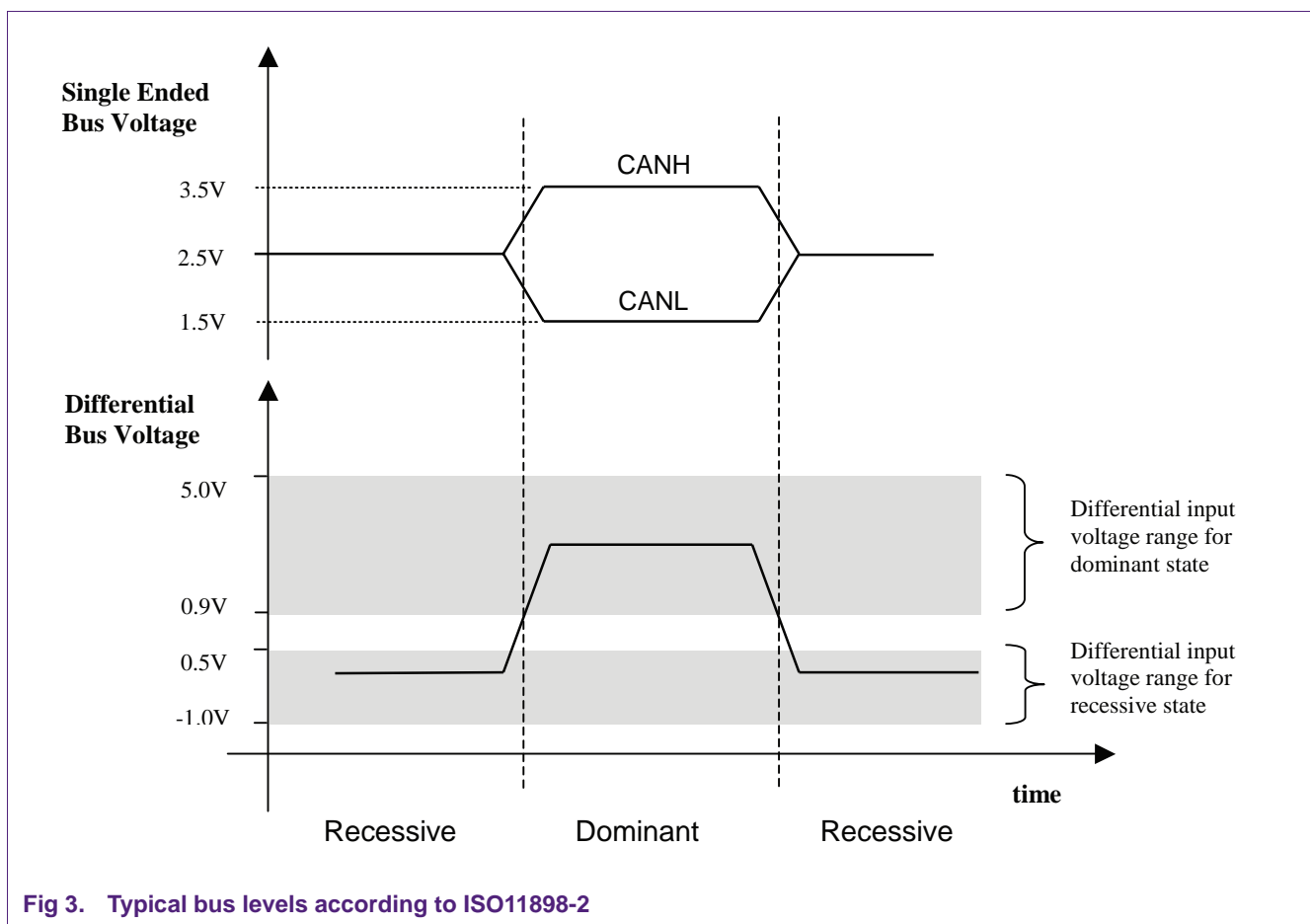
The block diagram in [Figure 2](#) describes the basic structure of an ECU. Typically an ECU (CAN-node) consists of a standalone transceiver and a host microcontroller with integrated CAN-controller, which are supplied by a voltage regulator. While the high speed CAN transceiver needs a +5 V supply, new microcontroller products are increasingly using lower supply voltages. In this case a dedicated voltage regulator is necessary for the microcontroller. The protocol controller is connected to the transceiver via a serial data output line (TXD) and a serial data input line (RXD). The transceiver is attached to the bus lines via its two bus terminals CANH and CANL, which provide differential receive and transmit capability. In the case of the TJA1041 there is an additional INH signal line (indicated in [Figure 2](#)) controlling the voltage regulator. Leaving control over the voltage regulator(s) for V_{CC} and µC supply voltage to the TJA1041(A) allows for an extremely low ECU quiescent current.

The CAN controller outputs a serial transmit data stream to the TXD input of the transceiver. An internal pull-up function within the TJA1041 sets the TXD input to logic HIGH i.e. the bus output driver is passive in open circuit condition. In the recessive state the CANH and CANL pins are biased to a voltage level of V_{CC}/2. If a logic LOW-level is applied to TXD, this activates the bus output stage, generating a dominant state on the

bus line. The output driver CANH provides a source output from V_{CC} and the output driver CANL a sink output towards GND. This is illustrated in [Figure 4](#) showing the block diagram of the TJA1041(A).

The bus stays in recessive state if no bus node transmits a dominant bit. If one or multiple bus nodes transmit a dominant bit, then the bus lines enter the dominant state overriding the recessive state (wired-AND characteristic).

The receiver converts the differential bus signal to a logic level signal, which is output at RXD. The serial receive data stream is provided to the bus protocol controller for decoding. The receiver comparator is always active i.e. it monitors the bus while the bus node is transmitting a message. This is required to support the non-destructive bit-by-bit arbitration scheme of CAN.



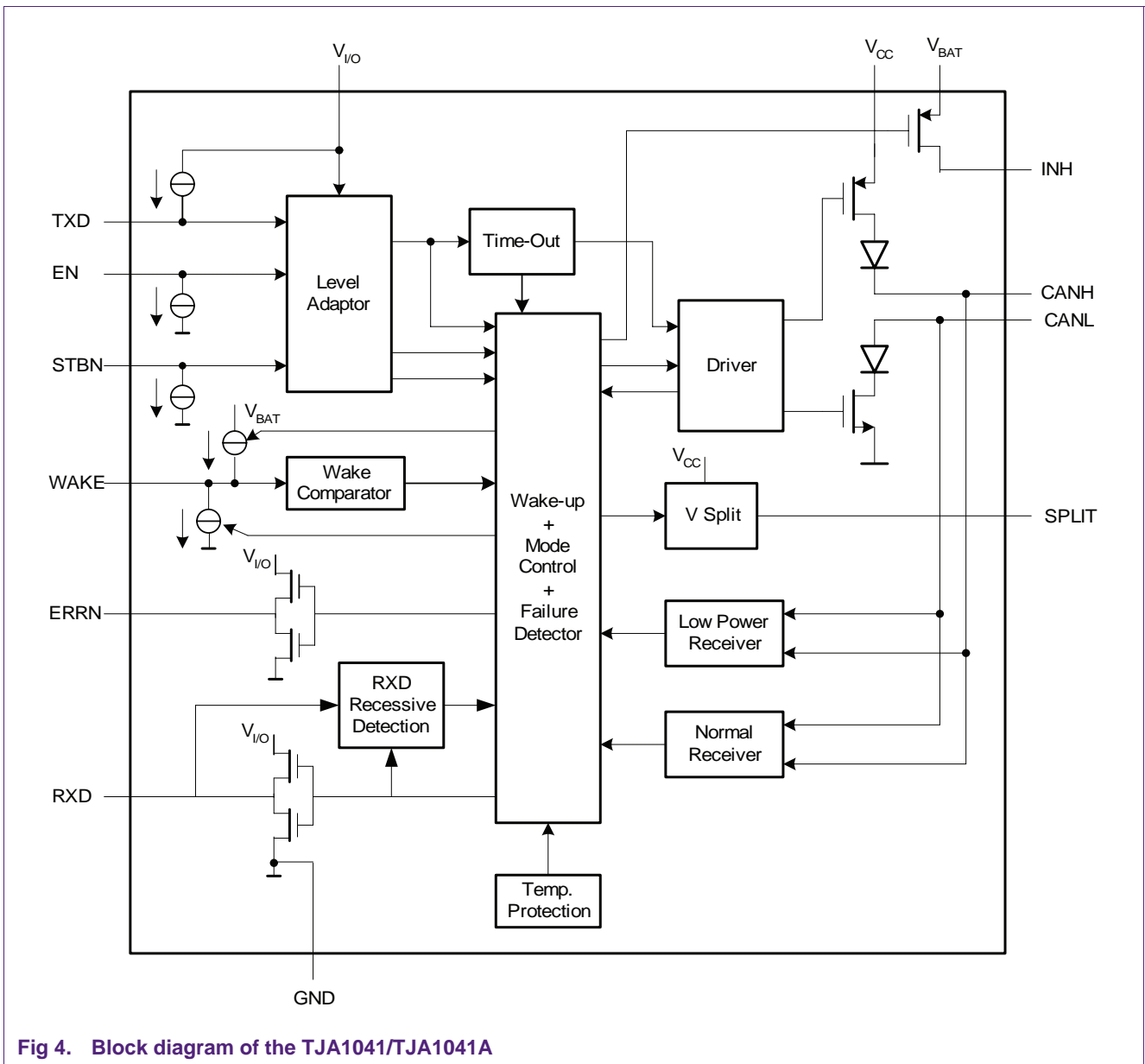


Fig 4. Block diagram of the TJA1041/TJA1041A

3. Target applications for TJA1041/TJA1041A

The TJA1041(A) high speed CAN transceiver is the ideal choice for applications which require high data throughput (up to 1 Mbit/s), bus diagnosis and enhanced low-power management. While the focus of the high speed CAN bus was mainly on Powertrain applications, particularly the low-power management of the TJA1041 enables the High-Speed CAN bus also for other in-vehicle multiplexing tasks like body multiplexing and ITS data bus [Ref. 10](#).

From an ECU power management point of view, four different application fields (type A to D) can be distinguished for high speed CAN, as illustrated in [Figure 5](#).

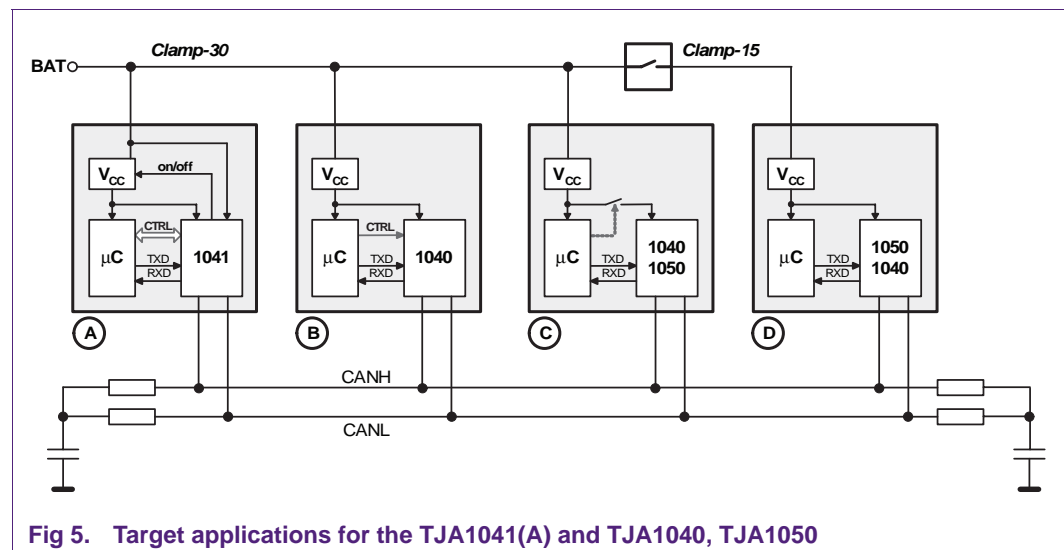


Fig 5. Target applications for the TJA1041(A) and TJA1040, TJA1050

Type A — Applications, which have to be available all time, even when the car is parked and ignition-key is off, are permanently supplied from a permanent battery supply line, often called “Clamp-30”. However, those nodes need the possibility to reduce the current consumption for saving the battery by control of the local ECU supply (V_{CC}). These type A applications allow switching off the entire supply system of the ECU including the microcontroller supply while keeping the wake-up capability via CAN.

The TJA1041(A) is the first choice for these applications. It can be put into its Sleep mode (all V_{CC} supplies off), which allows reducing the total current consumption of the entire ECU down to typically 20 μA , while keeping the capability to receive wake-up events from the bus and to restart the application.

Type B — Those applications, which need an always-active microcontroller, are permanently supplied from the battery supply line “Clamp-30” using a continuously active V_{CC} supply. In order to reduce the ECU power consumption, the transceiver needs to be set into a mode with reduced supply current while the V_{CC} stays active.

Here the Standby mode of the TJA1040 offers the best choice. During Standby mode the device reduces the V_{CC} supply current to a minimum, while still monitoring the CAN bus lines for bus traffic.

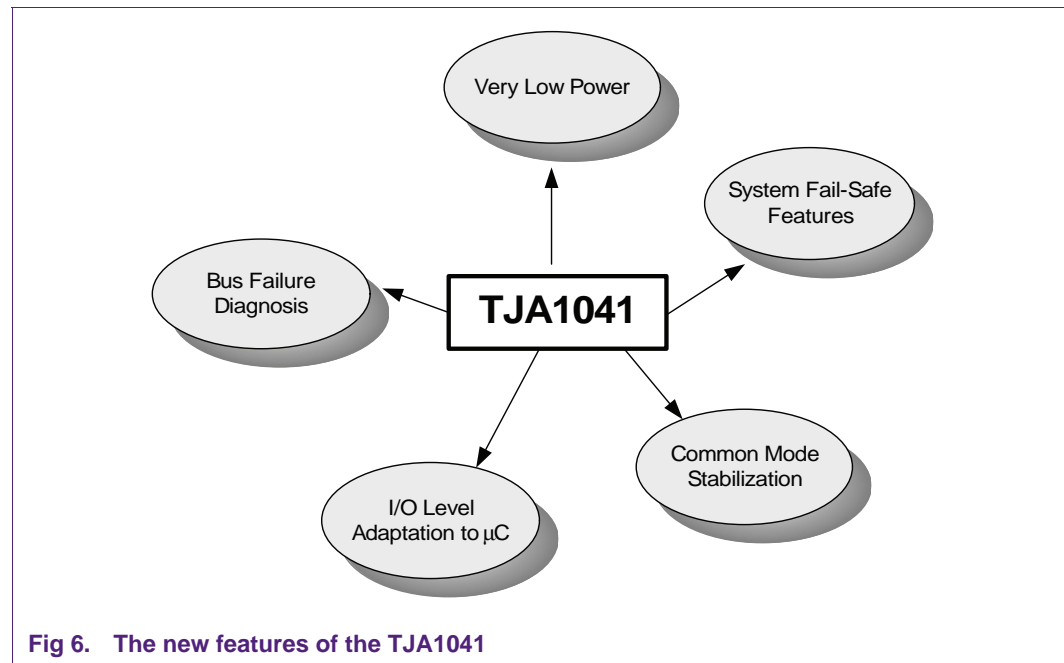
Type C — Dedicated applications, which need an always-active microcontroller and therefore are permanently supplied from the Clamp-30 line, additionally come with a microcontroller controlled transceiver voltage supply. In contrast to type B applications, further current can be saved, because the transceiver becomes completely un-powered by microcontroller control. These applications require absolute passive bus behavior of

the transceiver, while its voltage supply is inactive. This is important in order not to affect the remaining bus system, which might still continue communication. Most suitable for such kind of applications are the TJA1040 and TJA1050. While the TJA1050 allows some reverse current from the bus when becoming un-powered, the TJA1040 behaves absolutely passive to the bus.

Type D — Applications, which do not need to be available with ignition-key off, are simply switched off and become totally un-powered during ignition-key off. They are supplied from a switched battery supply line, often called “Clamp-15”. This supply line is only switched on with ignition-key on. Depending on system requirements, e.g. partial communication of the still supplied nodes during “ignition-key off”, these un-powered nodes need to behave passively towards the remaining bus, similar to type C applications. As for type C applications, it is recommended to use the TJA1040 or TJA1050 due to its passive behavior to the bus when becoming un-powered.

4. Main features

Today bus implementations call increasingly for low system power consumption, high system reliability, excellent EMC (Electromagnetic Compatibility) and flexible interfacing. The new features of the TJA1041(A), shown in [Figure 6](#), reflect this increasing demand on bus transceiver.



4.1 Low power management

Modern in-vehicle networking architectures require the availability of the high speed CAN bus even when ignition key is off. This requires permanently battery supplied ECUs with lowest current consumption. The low power management of the TJA1041(A) allows reducing the quiescent current consumption of an ECU to about typ. 20 μA . This current consumption is low enough to allow permanent battery supply of the transceiver and keeping wakeup capability via the bus. This way the system can react on local events as well as on CAN messages, resulting in wakeup of the complete bus system.

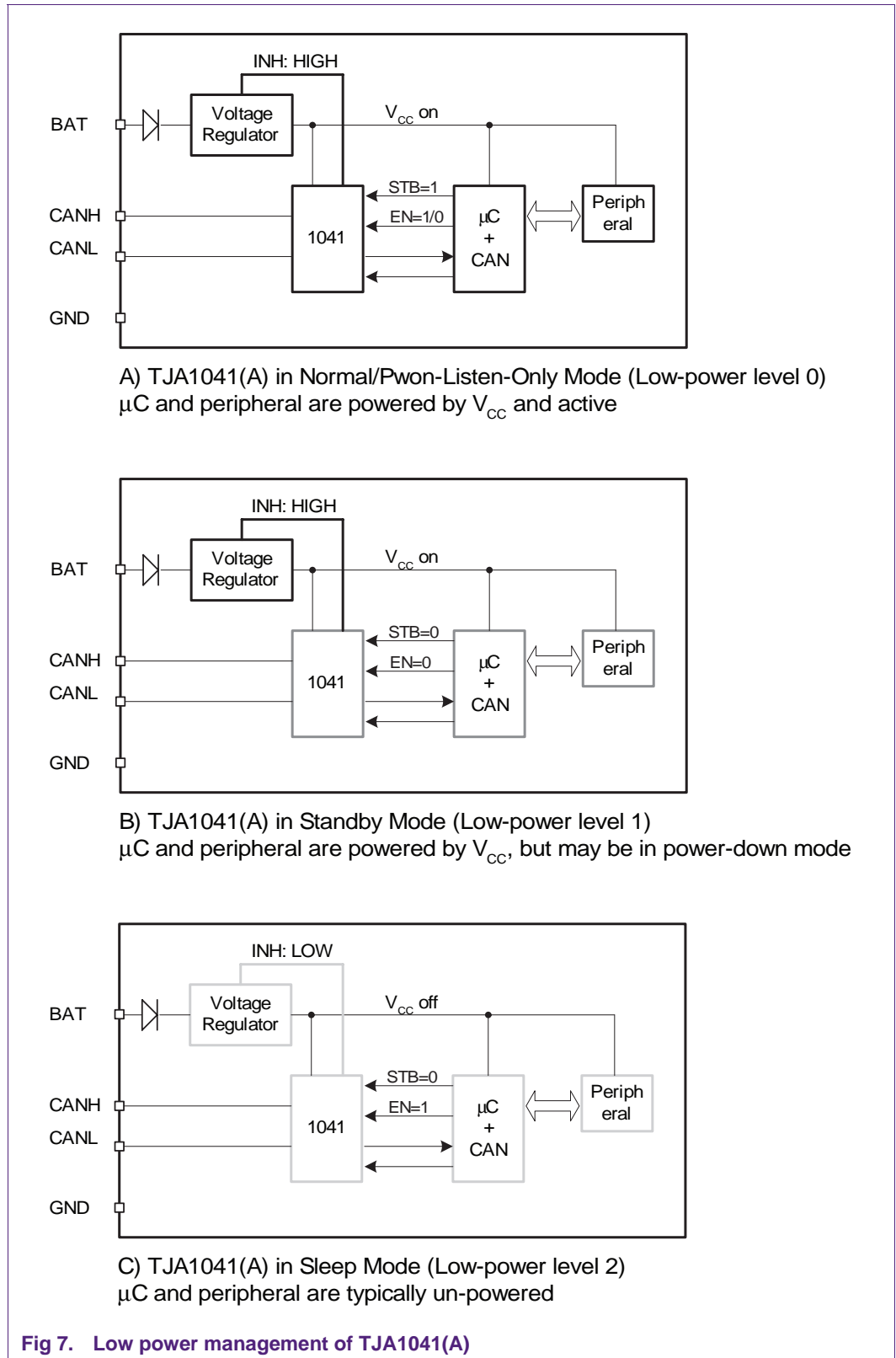
The operating modes of the TJA1041(A) (Normal, Pwon/Listen-Only, Standby, Sleep, Goto-Sleep Command) establish a low power management with three different levels as sketched in [Figure 7](#) and [Table 1](#). In level 0 the ECU components (voltage regulator, microcontroller, transceiver, peripherals) are active and powered. The TJA1041(A) is either in Normal or Pwon/Listen-Only mode. The transceiver and the host microcontroller are powered by the active V_{CC} supply.

The next level of low power, level 1, is achieved with the TJA1041(A) operating in Standby mode. The microcontroller, transceiver and peripherals are still powered by the active V_{CC} supply, but the functionality is often reduced to a minimum in order to save current. In the case of the TJA1041(A) the function is reduced to detection of wakeup events only. Transmit and receive function as provided in Normal mode is not available. The host microcontroller is often put in a power-down condition in order to save additional current.

The low power level 2 is associated to the Sleep mode of the TJA1041(A). In Sleep mode the external voltage regulator(s), supplying the transceiver and host microcontroller, is (are) typically switched off via the INH output signal of the transceiver. The V_{CC} supply for the transceiver and microcontroller is not available. While the host microcontroller and peripherals are completely un-powered, the TJA1041(A) keeps powered via the battery supply pin V_{BAT} . This supply is needed to ensure wakeup capability either via the bus or via a local wakeup event. The low power level 2 guarantees the lowest current consumption of a node.

Table 1. Characteristics of the different low power levels

Low power level	Operating mode	V_{CC} supply	μC	Node power consumption
Level 0 (Bus active)	Normal, Pwon/Listen-Only	Active	Powered	Normal
Level 1	Standby	Active	Powered	Low
Level 2	Sleep	Off	Un-powered	Very low



4.2 Bus failure diagnosis

The TJA1041(A) can detect short circuits on the bus wires and signal them to the host microcontroller. While physical bus failures normally lead to interruption of bus communication, there are certain bus failures that are tolerated within the physical layer of high speed CAN. Without the bus failure diagnosis feature of the TJA1041(A) the application microcontroller would not have a chance to become aware of those bus failures. Apart from increasing current consumption, those bus failures are responsible for poor EMC performance.

4.3 System fail-safe features

The system fail-safe features of the TJA1041(A) aim to keep the impact of possible local failures, like pin short-circuits, confined to the corrupted node only. After detection of a local failure, appropriate measures are taken to keep the remaining bus operable as long as possible. There are protections against TXD Dominant Clamping, TXD/RXD Short Circuit, RXD Recessive Clamping and Bus Dominant Clamping.

4.4 Common mode stabilization

The TJA1041(A) provides means for common mode stabilization by offering a low-impedance voltage source of nominal $V_{CC}/2$ at the pin SPLIT. This feature helps to stabilize the bus common mode voltage, especially with leakage currents on the bus. Such leakage currents may occur in presence of un-powered nodes during ignition-off. As a result this feature can improve the EMC performance in presence of unpowered ECUs. (see also [Section 6.1.11](#))

4.5 I/O level adaptation to host controller supply voltage

The I/O level adaptation of the TJA1041(A) allows the transceiver to be interfaced directly to any microcontroller with a typical supply voltage between 2.8V and 5V, without need for extra glue logic between transceiver and microcontroller.

The TJA1041(A) provides a continuous threshold level adaptation for the interface pins to the microcontroller down to a microcontroller supply voltage of 2.8 V [Ref. 1](#). For this purpose the host controller supply voltage is connected to the transceiver pin V_{IO} to provide the reference voltage for the input/output interface. It defines the ratiometric digital input threshold for TXD, EN and STBN and the HIGH-level output voltage for RXD and ERRN.

5. Operating modes

The TJA1041(A) provides five different operating modes, which are controlled by the input pins STBN and EN. The reference state diagram for the operating modes can be found in the data sheet [Ref. 1](#). In the case of an undervoltage condition on the pin V_{CC} or V_{IO} , the transceiver is forced into Sleep mode, overruling the current mode selection at the pins STBN and EN. In the case of an undervoltage condition on the pin V_{BAT} the transceiver is forced into Standby mode.

Depending on the operating mode the transceiver shows different behavior for the receiver and bus driver as well as on output pins like ERRN and RXD. [Table 1](#) summarizes the characteristics in each operating mode.

5.1 Normal mode

For CAN communication the Normal mode is chosen. The digital bit stream input at TXD is transferred into corresponding analog bus signals. Simultaneously, the transceiver monitors the bus, converting the analog bus signals into the corresponding digital bit stream output at RXD. The external voltage regulator is active, the bus lines are biased to $V_{CC}/2$ and the transmitter is enabled. The Normal mode is entered setting STBN to HIGH and EN to HIGH level.

5.2 Pwon/Listen-only mode

In general the Pwon/Listen-Only mode has two different functions. First, it realizes a Listen-Only behavior. The node is only allowed to receive messages from the bus but not to transmit onto the bus. The digital bit stream from the CAN-controller at TXD is simply ignored. In this way a node can be prevented from influencing the bus.

Secondly, the Pwon/Listen-Only mode provides the Local Failure flag and PWON flag at the pin ERRN, which can be read by the microcontroller. For flag signalling at the pin ERRN refer to [Section 7](#). The Pwon/Listen-Only mode is entered setting STBN to HIGH and EN to LOW level.

5.3 Standby mode

Standby mode is used to achieve low power level 1. Power consumption of the TJA1041(A) is significantly reduced compared to Normal or Pwon/Listen-Only mode. In Standby mode the TJA1041(A) is not capable of transmitting and receiving regular CAN messages. However, the TJA1041(A) monitors the bus for CAN messages. Whenever a wakeup pattern is detected on the bus, indicating bus traffic, the internal wakeup flag is set. The TJA1041(A) can also receive a local wakeup via the pin WAKE. On detection of a remote or local wakeup the internal Wakeup flag is set. In Standby mode this flag is output at the pins ERRN and RXD. To reduce the current consumption as far as possible the bus is terminated to GND rather than biased to $V_{CC}/2$ as in Normal or Pwon/Listen-Only mode. Standby mode is selected setting STBN to LOW and EN to LOW level.

5.4 Sleep mode

Sleep mode is used to achieve low power level 2. While the transceiver current consumption is the same as in Standby mode, it allows further reduction of the system current consumption by switching off the external voltage regulator (V_{CC} supply) for the transceiver, host microcontroller etc.

The only difference between Sleep and Standby mode concerns the pin INH. It provides a battery related open drain output to control one or more external voltage regulators. In Sleep mode the pin INH is set floating compared to a HIGH signal (V_{BAT} -based) in all other modes (also Standby mode), typically disabling the voltage regulator(s) for the transceiver and microcontroller. While the microcontroller is completely un-powered (no V_{CC} supply), the TJA1041(A) keeps partly alive via its battery supply. It allows the transceiver to monitor the bus for CAN messages. In fact, the transceiver is the device controlling autonomously the V_{CC} supply for the ECU.

Wakeup from Sleep mode is generally possible via two channels:

- Wakeup via a dominant bus state

- Local wakeup via an edge at pin WAKE

On wakeup, the pin INH goes HIGH enabling the external voltage regulator(s) again. The wakeup flag is set for a local or remote wakeup. It is reflected at the pins ERRN and RXD. As in Standby mode, the bus lines CANH and CANL are terminated to GND. [Table 2](#) summarizes the characteristics of the TJA1041(A) in the different operating modes.

The only way to put the TJA1041(A) into Sleep mode is using the Goto Sleep Command mode (STBN to LOW, EN to HIGH). If it is selected for longer than the minimum hold time of go-to-sleep command $t_{h(min)}$ [Ref. 1](#), the transceiver is automatically forced into Sleep mode switching the pin INH to floating.

A mode transition from Sleep mode to any other mode via STBN and EN is possible only if the supply voltage V_{CC} and V_{IO} were present all time during Sleep mode. Once a V_{CC} or V_{IO} under-voltage is detected, mode control via STBN and EN is disabled for fail-safe reasons. This feature prevents the microcontroller from continuously waking up the transceiver via STBN and EN in the case of a V_{CC} or V_{IO} under-voltage being detected by the transceiver.

A continuous situation, where one part of the nodes is in Normal or Pwon/Listen-Only mode while the other part is in Standby or Sleep mode, should be avoided due to the different bus biasing in these modes. Otherwise a continuous DC common mode current would flow from one part to the other.

5.5 Go-to Sleep Command mode

The Go-to-Sleep Command mode has the meaning of a command rather than the meaning of a typical operating mode. It is used to put the TJA1041(A) into Sleep mode. Due to the spread of the minimum hold time of go-to-sleep command $t_{h(min)}$ [Ref. 1](#) the Go-to Sleep Command mode must be actually selected for longer than the maximum value in order to make sure the Sleep mode is entered reliably. Immediately after selecting the Go-to Sleep Command mode the transmitter is disabled, the bus lines are terminated to GND and the Wakeup flag information is signalled at the pins ERRN and RXD. The Go-to Sleep Command mode is selected with STBN to LOW and EN to HIGH level.

Remark: the Go-to Sleep Command might become overruled by a wake-up event, if this wake-up event occurs simultaneously with the Go-to Sleep Command. In this case, the wake-up will be signalled on RXD and ERRN as desired, while INH stays active HIGH.

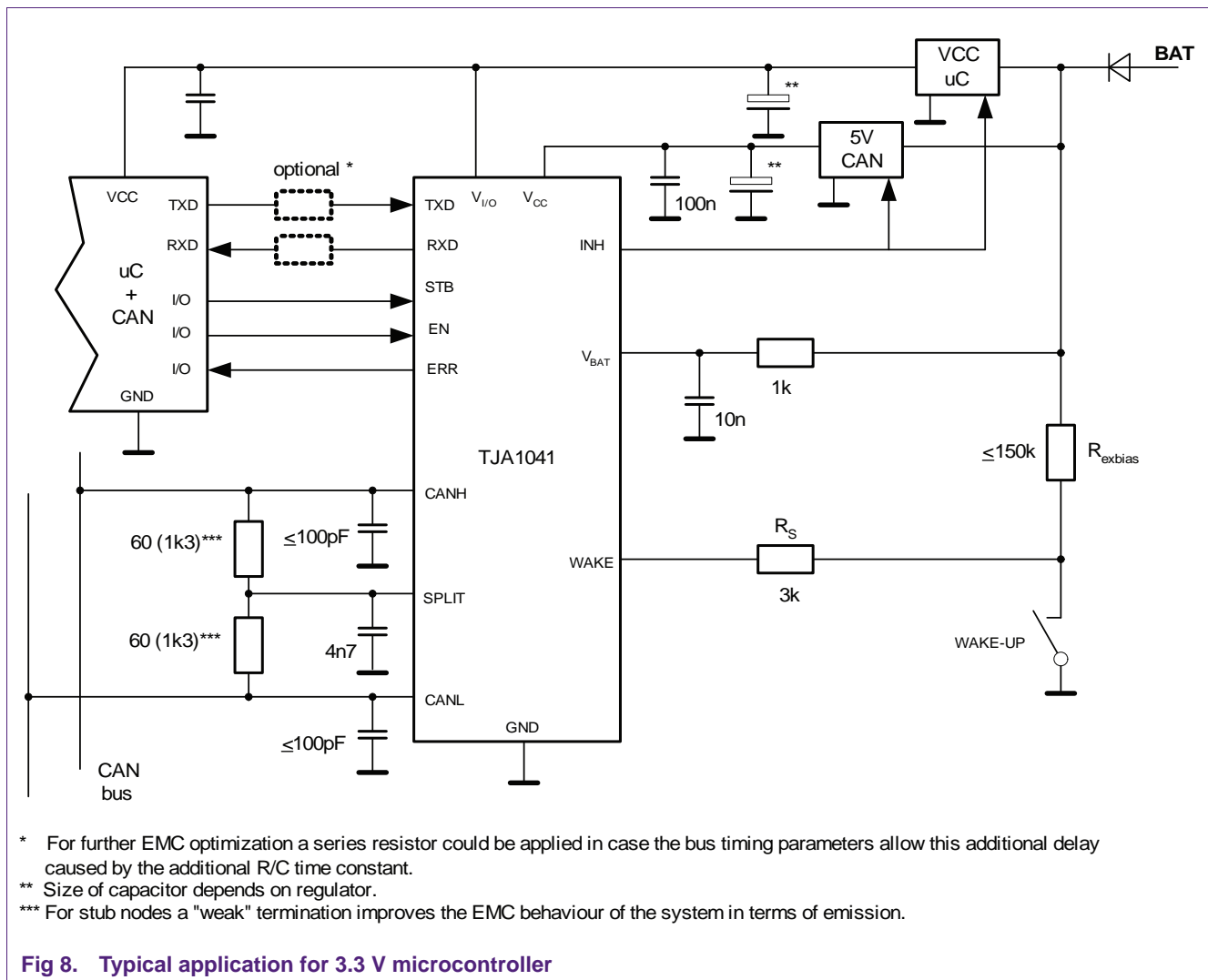
Table 2. Characteristics of the different modes

Operating mode	STBN	EN	ERRN-pin		RXD-pin		Bus bias	INH-pin
			Low	High	Low	High		
Normal	1	1	Bus Failure flag set [1] Wakeup Source flag; local wakeup detected [2]	Bus Failure flag reset [1] Wakeup Source flag; remote wakeup detected [2]	Bus dominant	Bus recessive	$V_{CC}/2$	V_{BAT}
Pwon/ Listen-only	1	0	PWON flag set; [3] Local Failure flag set [4]	PWON flag reset; [3] Local Failure flag reset [4]	Bus dominant	Bus recessive	$V_{CC}/2$	V_{BAT}
Go-to Sleep Command	0	1	Wakeup flag set [5]	Wakeup flag reset [5]	Wakeup flag set [5]	Wakeup flag reset	GND	V_{BAT}
Standby	0	0						V_{BAT}
Sleep; [6]	0	X						float

- [1] Valid after the fourth dominant to recessive edge at TXD after entering the Normal mode (each dominant period should be at least 4 μ s).
- [2] Valid before the fourth dominant to recessive edges at TXD after entering the Normal mode.
- [3] Valid if V_{IO} and V_{CC} are present and coming from Sleep, Standby or Go-To-Sleep Command mode.
- [4] Valid if V_{IO} and V_{CC} are present and coming from Normal mode.
- [5] Valid if V_{IO} and V_{CC} are present .
- [6] Transceiver will enter the Sleep mode only if the Go-To-Sleep Command mode was selected longer than the hold time of go-to-sleep command ($t_{h(min)}$) or by an under-voltage detection on V_{IO} or V_{CC} .

6. Hardware application of the TJA1041(A)

Figure 8 shows how to integrate the TJA1041(A) within a typical application. The application example assumes a 3.3 V supplied host microcontroller. There is a dedicated 5 V regulator supplying the TJA1041(A) transceiver and a dedicated 3.3 V regulator supplying the microcontroller. Both voltage regulators are controlled via the INH output of the transceiver, so that in Sleep mode both voltage regulators are switched off. Furthermore, the application example makes use of the pin WAKE for local wakeup possibility, connecting it to a low-side switch.



6.1 Pin description

6.1.1 Pin V_{BAT}

The battery supply ensures the local and remote wakeup capability of the TJA1041(A) when the V_{CC} supply is switched off during Sleep mode. Nevertheless the current consumption I_{BAT} via this pin is very low [Ref. 1](#). It is recommended to place a series resistor of 1 kΩ into the battery supply line of the transceiver for enhanced protection

against automotive transients. Given the max. supply current I_{BAT} of 40 μ A at V_{BAT} , a voltage drop of 40 mV must be taken into account when calculating the minimum battery operating voltage. In addition, a capacitor of about 10 nF, closely connected to the V_{BAT} pin and forming a low-pass filter in conjunction with the series resistor, can be used for enhanced transient protection.

6.1.2 Pin V_{CC}

The V_{CC} supply provides the current needed for the transmitter and receiver of the TJA1041(A). The V_{CC} supply must be able to deliver current of 65 mA in average for the transceiver (see [Section 15.2](#)). Using a linear voltage regulator, it is recommended to stabilize the output voltage with a bypass capacitor of about 20 μ F (see [Section 15.2](#)). This type of capacitor should be connected at the output of the voltage regulator. In addition, a second capacitor should be connected as close as possible between pin V_{CC} and GND of the transceiver. Its function is to buffer the V_{CC} supply voltage, especially during fast load changes at a transition from recessive to dominant. Recommended value is 47-100 nF. For reliability reasons it might be useful to apply two capacitors in series connection between V_{CC} and GND. A single shorted capacitor (e.g. damaged device) cannot short-circuit the V_{CC} supply.

6.1.3 Pin V_{IO}

Pin V_{IO} is connected to the μ C supply voltage to provide the proper voltage reference for the input threshold of digital input pins and for the HIGH voltage of digital outputs. Unlike other products on the market, the TJA1041(A) provides a continuous level adaptation from as low as 2.8 V to 5 V. The level adaptation applies to all interface pins between the microcontroller and the transceiver, i.e. TXD, EN, STBN (input pins) and RXD, ERRN (output pins). In Normal mode only a small current I_{IO} [Ref. 1](#) is drawn out of the V_{IO} supply. In Sleep mode no current will be drawn via this pin. If the pin V_{IO} is disconnected, an under-voltage condition on V_{IO} will be detected and the transceiver is forced into Sleep mode in order to provide defined fail-safe low-power system behavior.

6.1.4 Pin TXD

The transceiver receives the digital bit stream to be transmitted onto the bus via the pin TXD. When applied signals at TXD show fast slopes, it may cause a degradation of the EMC performance. In this case, it is recommended to place a series resistor of about 1 k Ω into the TXD line between transceiver and microcontroller. Along with pin capacitance this would help to smooth the edges to some degree. For high bus speeds (close to 1 Mbit/s) the additional delay within TXD has to be taken into account.

6.1.5 Pin RXD

The analog bit stream received from the bus is output at pin RXD for further processing within the CAN-controller. As with pin TXD a series resistor of about 1 k Ω can be used to smooth the edges at bit transitions. Again the additional delay within RXD has to be taken into account, if high bus speeds close to 1 Mbit/s are used.

6.1.6 Pin STBN/EN

The pins STBN and EN are used for mode control. They are typically connected to an output port pin of a microcontroller.

6.1.7 Pin ERRN

The pin ERRN is a push-pull output stage for signalling failure conditions to the microcontroller. It is typically connected to an input port pin of a microcontroller. (see [Ref. 1](#) for drive capability)

6.1.8 Pin CANH/L

The transceiver is connected to the bus via pin CANH/L. Nodes connected to the bus end must show a differential termination, which is approximately equal to the characteristic impedance of the bus line in order to suppress signal reflection. Instead of a one-resistor termination it is highly recommended using the Split Termination, illustrated in [Figure 9](#). EMC measurements have shown that the Split Termination can improve significantly the signal symmetry between CANH and CANL, reducing emission. Basically each of the two termination resistors is split into two resistors of equal value, i.e. two resistors of 60 Ω instead of one resistor of 120 Ω . The special characteristic of this approach is that the common mode signal, available at the centre tap of the termination, is terminated to ground via a capacitor. The recommended value for this capacitor is in the range of 4.7 nF and 47 nF.

As the symmetry of the two signal lines is crucial for the emission performance of the system, the matching tolerance of the two termination resistors should be as low as possible (desired: < 2 %).

Also depicted in [Figure 9](#), it is recommended to load the CANH and CANL pin each with a capacitor of about 100 pF close to the connector of the ECU. The main reason is to increase the robustness to automotive transients and ESD. The matching tolerance of the two capacitors should be as low as possible.

6.1.9 Pin SPLIT

In Normal and Pwon/Listen-Only mode the pin SPLIT provides an output voltage of $V_{CC}/2$. In all other modes the pin is in high-ohmic state. By simply connecting the pin SPLIT to the center tap of the Split Termination as shown in [Figure 9](#), DC stabilization of the common mode voltage is achieved.

In the case of unpowered nodes, leakage currents from the bus into the transceiver may force the common mode voltage to drop below $V_{CC}/2$ during recessive state. The DC stabilization aims to oppose this degradation and helps improving the emission performance. With no significant leakage currents from the bus, the pin SPLIT can be left open.

According to the data sheet [Ref. 1](#) the maximum impedance of the voltage source can be calculated to 2000 Ω .

6.1.10 Pin WAKE

The pin WAKE can be used to signal a local wakeup event to the transceiver. Like the Fault-tolerant CAN Transceiver TJA1054 [Ref. 5](#) a signal change of sufficient length at the pin WAKE generates a local wakeup. That means both a rising and a falling edge can be applied to launch a local wakeup. Typically, a low-side switch is used at the pin WAKE as shown in [Figure 9](#). The series resistor R_S is for protection and limits the output current when the transceiver has lost its ground connection, while the low-side switch is closed. The pull-up resistor R_{exbias} is needed to provide a sufficient current for the switch contacts. More information on the values for R_S and R_{exbias} is given in [Section 7.2.1](#).

6.1.11 Pin INH

The intention of the pin INH is to control one or more voltage regulators within the ECU. In [Figure 9](#) two voltage regulators, one 5 V regulator for the transceiver and one 3.3 V regulator for the microcontroller, are controlled via the INH output of the transceiver as an example.

The pin INH provides a battery related open drain output. During Sleep mode it is floating. Due to the typical pull-down behavior of the Inhibit input pin of common voltage regulators, this results in a LOW signal on the Inhibit input, typically disabling the voltage regulator(s). In all other operation modes the pin INH is actively pulled to battery voltage, enabling the external voltage regulator(s). The load resistance at the pin INH shall not be lower than 10 kΩ for 12 V battery systems. If the pin INH is not used for voltage regulator control, it can be left open.

6.2 Application of common mode choke

A common mode choke provides high impedance for common mode signals and low impedance for differential data signals. Due to this, common mode signals, either produced by RF noise or by the transceiver itself, get effectively attenuated while passing the choke. In fact, a common mode choke helps to reduce emission and to improve immunity against common mode disturbances.

Former transceiver devices usually needed a common mode choke to fulfill the stringent emission and immunity requirements of automotive when using unshielded twisted-pair cable. The TJA1041(A) has the potential to build in-vehicle bus systems without chokes. Whether a choke is needed or not finally depends on the specific system implementation like the wiring harness and the symmetry of the two bus lines (matching tolerances of resistors and capacitors).

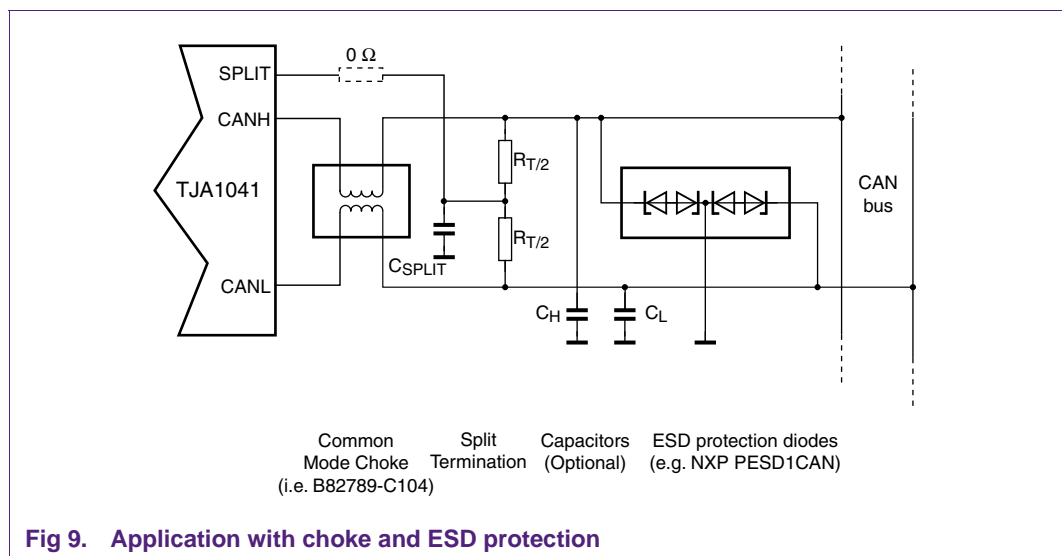


Fig 9. Application with choke and ESD protection

Besides RF noise reduction, stray inductance (non-coupled portion of inductance) may establish a resonant circuit together with pin capacitance. This can result in unwanted resonance oscillations between the bus pins and the choke, both for differential and common mode signals, and in extra emission around the resonant frequency. To avoid

such oscillations, it is highly recommended to use only chokes with a stray inductance lower than 500 nH. Bifilar wound chokes typically show an even lower stray inductance. As shown in [Figure 9](#) the choke should be placed near to the transceiver.

6.3 ESD protection

The TJA1041(A) is designed to withstand ESD pulses of up to 6 kV according to the human body model at the bus pins CANH, CANL and pin SPLIT and typically does not need further external protection methods. Nevertheless, if much higher protection is required, external clamping devices can be applied to the CANH and CANL line.

NXP offers a dedicated protection device for the CAN bus, providing high robustness against ESD and automotive transients. The PESD1CAN ESD protection diode [Ref. 13](#), featuring a very fast diode structure with very low capacitance (typ. 11 pF), is compliant with IEC61000-4-2 (level 4), allowing air and contact discharge of more than 15 kV and 8 kV, respectively. Tests at an independent test house have confirmed more than 20 kV ESD robustness for ECUs equipped with the PESD1CAN diode and a choke. To be most effective the PESD1CAN diode should be placed close to the ECU connector as shown in [Figure 9](#) while the choke should be placed near to the transceiver.

6.4 PCB layout rules

Following guidelines should be considered for the PCB layout.

- When a common mode choke is used, it should be placed close to the transceiver bus pins CANH and CANL.
- The PCB tracks for the bus signals CANH and CANL should be routed close together in a symmetrical way. Its length should not exceed 10 cm.
- Suppressor diodes or varistors for ESD protection should be connected close to the ECU connector bus terminals.

7. Wakeup detection

There are in general two possibilities to wake up the transceiver, either via the bus or via the WAKE pin. On detection of a wakeup event the Wakeup flag is set and signalled at RXD and ERRN.

7.1 Wakeup via bus

The only difference between the TJA1041 and TJA1041A concerns the bus wakeup mechanism. The TJA1041 detects a bus wake-up request when the bus remains in dominant state for at least 5 μ s. In contrast to that, the TJA1041A detects a bus wake-up request when the bus shows two dominant phases of at least 5 μ s duration, with each dominant phase followed by a recessive phase of at least 5 μ s. [Figure 10](#) illustrates the bus wake-up pattern requirements for the TJA1041 and TJA1041A.

The enhanced bus wakeup detection offers improved robustness against unwanted wakeup in presence of bus failures, especially for large networks. There will be no unwanted bus wake-up due to a BAT-to-CANH short-circuit or CANL wire interruption, while the system is entering Bus Sleep.

At a data rate of 500 kbit/s, a single arbitrary CAN data frame is not necessarily sufficient to launch a remote wake-up with the enhanced wake-up pattern. Here, two consecutive arbitrary CAN data frames are needed to reliably launch a remote wake-up. At 125 kbit/s data rate, any CAN data frame on the bus will lead to a remote wake-up of the TJA1041A transceiver.

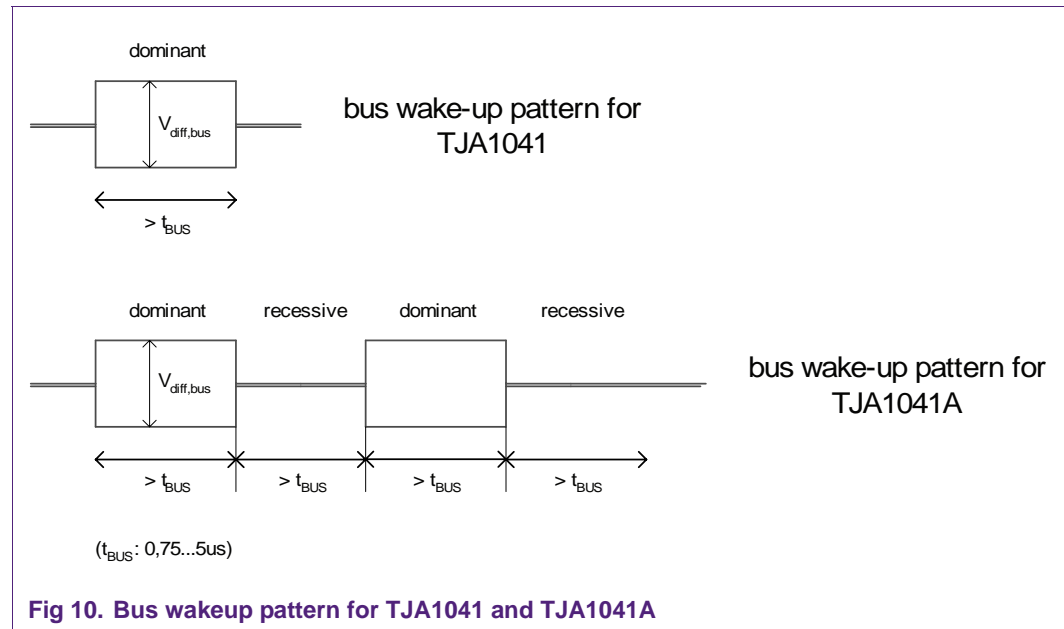


Fig 10. Bus wakeup pattern for TJA1041 and TJA1041A

7.2 Wakeup via WAKE pin

The pin WAKE can be used to signal a local wakeup event to the transceiver. Like the Fault-tolerant CAN Transceiver TJA1054 [Ref. 5](#) a signal change of sufficient length at the pin WAKE generates a local wakeup. While the TJA1054 features an internal pull-up to battery voltage to allow use of a low-side switch, the pin WAKE of the TJA1041(A) features variable biasing. Depending on the external biasing the internal one switches from GND to battery level or vice versa. [Figure 11](#) illustrates the biasing concept of the pin WAKE along with different external switching circuits.

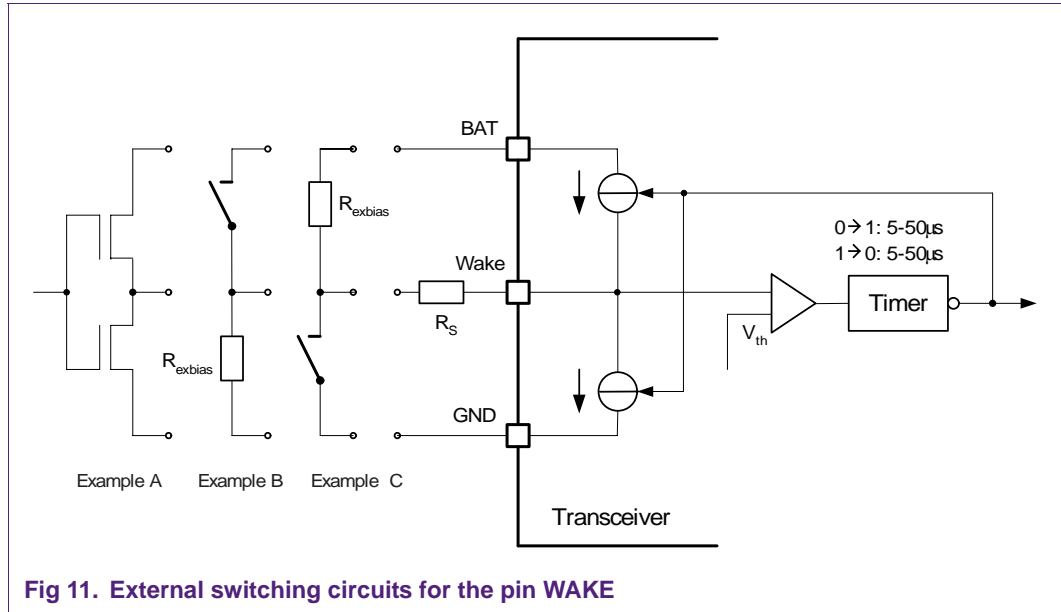


Fig 11. External switching circuits for the pin WAKE

If a voltage higher than the Wakeup Threshold Voltage $V_{th(WAKE)}$ [Ref. 1](#) is held at the pin WAKE for longer than the maximum time t_{WAKE} [Ref. 1](#), the internal biasing (current source) will switch reliably to battery level if the pin was at LOW level before. Similarly, if a voltage lower than this value is held for longer than the max. t_{WAKE} time, the internal biasing (current source) switches reliably to GND if the pin was at HIGH level before. The internal biasing is adapted automatically to the external biasing conditions. This concept allows using a low-side switch as well as a high-side switch or a V_{BAT} based push-pull stage without forcing undesired bias currents while there is no wakeup event.

In the case of a low-side switch, both the resistor R_{exbias} and the internal current source provide a pull-up to V_{BAT} . In order to launch a local wakeup the external switch has to be closed producing a negative pulse at the pin WAKE. The negative pulse passes the internal timer and releases a wakeup reliably if the pulse is longer than the maximum value of t_{WAKE} [Ref. 1](#). Along with passing the timer the bias switches to GND. After releasing the low-side switch the external pull-up resistor switches the internal bias back to V_{BAT} . The resistor R_{exbias} determines the current through the external switch when it is closed and is needed to guarantee a proper switch contact.

If pin WAKE is not used, connect the pin directly to ground level.

7.2.1 Dimensioning of R_S and R_{exbias}

The purpose of the series resistor R_S is to protect the transceiver if the ECU has a loss of ground situation while the wakeup switch still is connected to a proper GND. The minimum required series resistor is determined by the expected maximum battery supply voltage $V_{BAT,max}$ and the maximum allowed current at pin WAKE of 15 mA. The resistor should make sure that the current does never exceed this level. The minimum required series resistor R_S can be calculated by:

$$R_{S,min} = \frac{V_{BAT,max}}{I_{Wake,max}} \tag{1}$$

Assuming that V_{BAT} will not exceed 40 V DC, the series resistor should have a value of 3 k Ω .

The resistor R_{exbias} is needed to turn the bias to its default state after the external switch has been released. That defines an upper limit for the resistor value. For example, with a low-side switch the resistor R_{exbias} together with the series resistor R_S must pull the pin WAKE above the switching threshold of the pin WAKE. The equation for determining the upper limit for R_{exbias} is:

$$(R_{exbias} + R_S) \cdot I_{Pull,max} < V_{BAT} - V_{th(Wake),max} \quad (2)$$

With the maximum pull-down (pull-up) current of 10 mA and the maximum threshold of $V_{th(WAKE)}$, the theoretical upper limit for R_{exbias} calculates to about 180 k Ω . A typical value is 20 k Ω .

8. Flag signaling

The TJA1041(A) provides five different flags to be signalled to the microcontroller. The status of the flags can be read by the microcontroller via the pin ERRN. Which flag is actually signalled on the pin ERRN depends on the current operating mode and on the history. [Figure 12](#) shows the flag signaling of the pin ERRN.

Notice that when switching from one mode to another, it takes some time until the “new” flag is signaled at ERRN. To read pin ERRN with the application software, after a mode transition has been performed, first introduce a wait time in the software of at least 10 μ s.

8.1 Wakeup flag

A wakeup event from the bus or the pin WAKE sets the Wakeup flag only if the wakeup event is received while the TJA1041(A) is in Sleep, Standby or Go-to Sleep Command mode. In Normal or Pwon/Listen-Only mode any wakeup event is ignored. The Wakeup flag is signalled at the pin ERRN during Sleep, Standby and Go-to Sleep Command mode provided that V_{CC} and V_{IO} are present. A LOW level signals a wakeup request for the microcontroller, received either via the bus or via the pin WAKE. It is reset either when the Normal mode is entered or when there was a BAT-Under-voltage condition detected. As long as the Wakeup flag is set, a Go-to Sleep Command is simply ignored and a transition into Sleep mode is not possible. The Wakeup flag is also signalled at the pin RXD with the same polarity as described for the pin ERRN.

8.2 PWON flag

The PWON flag is signalled at the pin ERRN during Pwon/Listen-Only mode when coming from Standby, Sleep or Go-to Sleep Command mode. It is set to LOW level if there was a battery under-voltage condition. If the battery has been connected the first time to the pin V_{BAT} or if there was a temporary battery under-voltage condition, this flag is set. The PWON flag is reset once the Normal mode is entered. As long as the PWON flag is set, it is not possible to enter Sleep mode. After first battery supply the PWON flag is initialized to “set”, indicated by a LOW level at pin ERRN.

8.3 Wakeup source flag

Entering Normal mode, pin ERRN first reflects the Wakeup Source flag. A LOW level signals a local wakeup via the pin WAKE, whereas a HIGH level indicates a wakeup via the bus. The Wakeup Source flag is overwritten by the Bus Failure flag after the node has transmitted four recessive-to-dominant bit transitions in Normal mode. Since the application is controlling its own transmission behavior, the application has any time needed to read this Wakeup Source flag. The Wakeup Source flag is cleared and set to the default state HIGH whenever the Normal mode is left. After first battery supply the Wakeup-Source flag is initialized to “wakeup via bus”, indicated by HIGH level at pin ERRN.

8.4 Bus failure flag

After the transceiver has transmitted four recessive-to-dominant bit transitions with a dominant bit length of at least 4 ms, the Bus Failure flag overwrites the Wakeup Source flag. A LOW level indicates a short circuit condition on the bus. The Bus Failure flag is reset to default HIGH on leaving Normal mode. If there is no local wakeup meantime,

leaving and re-entering Normal mode forces pin ERRN to default state HIGH. Signalling the Bus Failure flag requires retransmission of at least four recessive-to-dominant bit transitions. Detection of bus failures does not lead to a change of transceiver operation. Active fault tolerance as known from the TJA1054 low speed CAN transceiver is not supported.

8.5 Local failure flag

Entering Pwon/Listen-Only mode from Normal mode, pin ERRN signals the Local Failure flag. A LOW level indicates those failures, which are associated with the local node only like

- TXD Dominant Clamping
- TXD/RXD Short Circuit
- RXD Recessive Clamping
- Bus Dominant Clamping
- Over-temperature Condition

For a detailed description of the detected local failures refer to [Section 10](#). If any of these local failures is present, this is indicated to the application by an active LOW signal. A more differentiated diagnosis is not supported. Along with setting the Local Failure flag, the transmitter is disabled because of fail-safe reasons, except for RXD Dominant Clamping detection. The Local Failure flag is reset and the transmitter enabled again either by forcing a transition into Normal mode or by receiving a dominant bit from the bus while TXD is recessive.

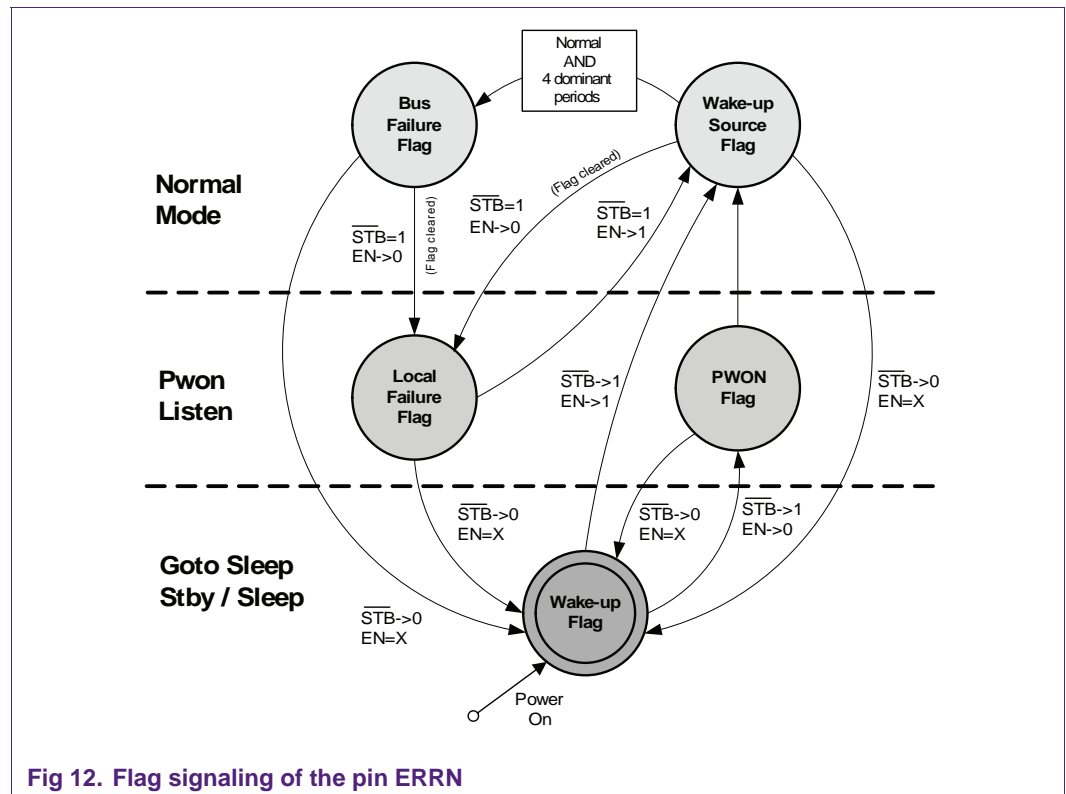


Fig 12. Flag signaling of the pin ERRN

9. Bus failure diagnosis

9.1 List of signaled bus failures

Assuming a bus load of nominal 60 Ω the following bus failure conditions are detectable by the TJA1041(A):

- CANH x BAT (communication still possible, “hidden” bus failure)
- CANH x V_{CC} (communication still possible, “hidden” bus failure)
- CANH x GND (communication not possible)
- CANL x BAT (communication not possible)
- CANL x V_{CC} (communication not possible)
- CANL x GND (communication still possible, “hidden” bus failure)

Listed short-circuits are reliably detected in the range 0 to 50 Ω . A short-circuit between CANH and CANL or line interruption failures are not detected. For analyzing the bus the node needs to actively transmit onto the bus. Before the Bus Failure flag becomes valid, the node must have transmitted at least four dominant sequences onto the bus each of at least 4 μ s length.

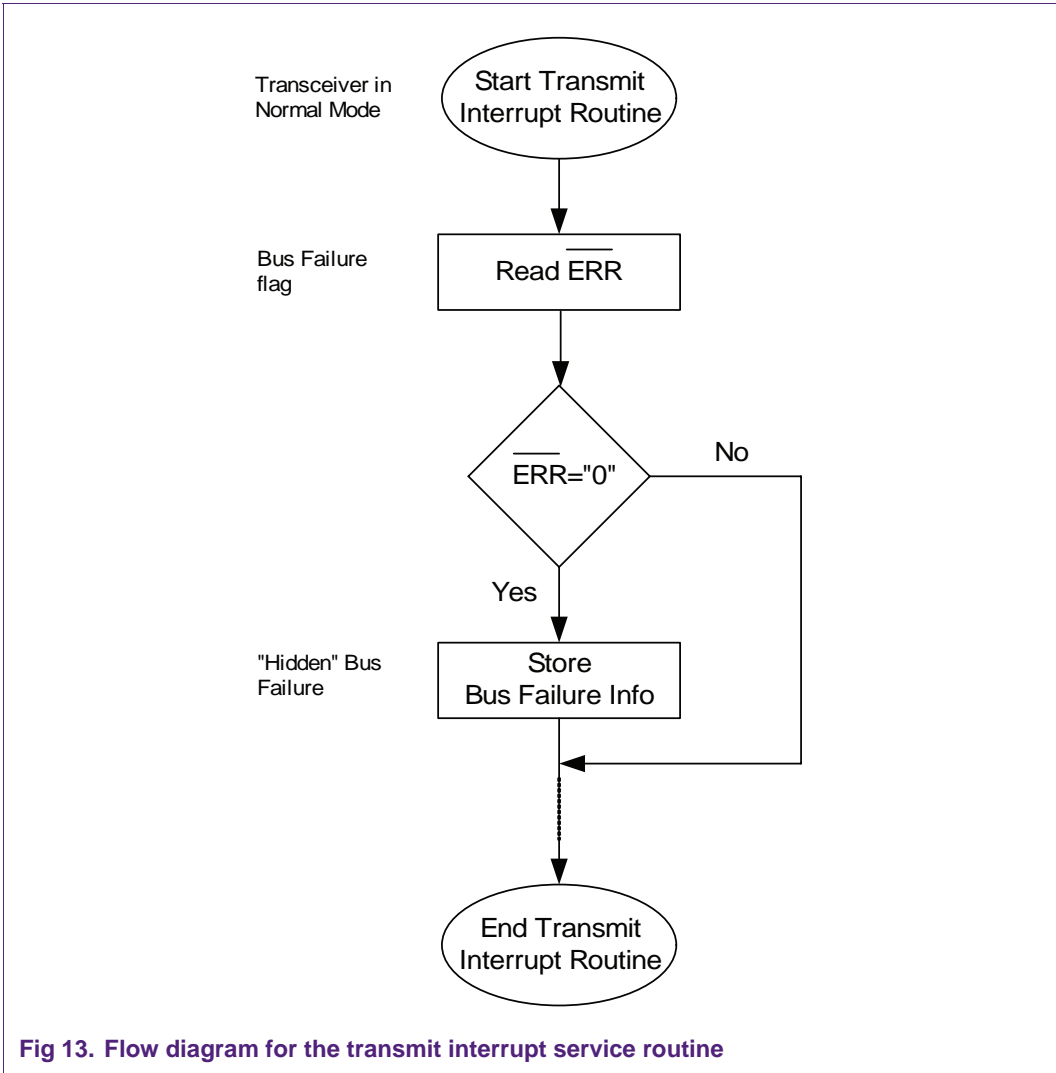
As already mentioned in [Section 4.2](#), the bus system performance suffers from hidden bus failure conditions in terms of EMC. The hidden bus failures are a short-circuit CANHxBAT, CANHxV_{CC} and CANLxGND. They are normally tolerated by the CAN High-Speed Physical Layer as long as the capacitive load on the bus is not too large, otherwise dominant periods on the bus would lengthen at the expense of recessive periods, possibly causing bit timing violations. Communication between nodes is still possible. Without additional diagnosis on physical layer level the microcontroller has no chance to get to know from those bus failures. The bus failure diagnosis aims to detect such failure conditions and to signal them to the application microcontroller.

9.2 How to read the bus failure flag

The Bus Failure flag is actually signalled at the pin ERRN. When entering Normal mode, pin ERRN first reflects the Wakeup-source flag. After four dominant periods of sufficient length have been transmitted, the Bus Failure flag gets active at the pin ERRN.

During arbitration, when more than one node may transmit simultaneously the bus failure measurement process may be distorted, resulting in unstable bus failure information. It is recommended that reading the Bus Failure flag from the microcontroller should take place at the end of the CAN frame only, e.g. within the transmit interrupt service routine. The read process should be completed before the transceiver sends the next CAN message. In order to be able to guarantee the four needed dominant periods each of more than 4 μ s length, a dedicated diagnosis message with appropriate payload may be helpful, especially for high bit rates.

A possible flow diagram for the transmit interrupt service routine is shown in [Figure 13](#). If reading of the pin ERRN indicates a LOW signal, a hidden bus failure must be present, because with bus failures, leading to complete corruption of communication, the transmit interrupt service routine would never be reached.



10. Local failure diagnosis

Local failures detected and signalled at the pin ERRN in Pwon/Listen-Only mode (when coming from Normal mode) include:

- TXD Dominant Clamping
- TXD/RXD Short Circuit
- RXD Recessive Clamping
- Over-temperature

On detection of one of these local failures, the Local Failure flag is set and the transmitter disabled. Failures listed here and information about Bus Dominant Clamping are not stored with the Local Failure flag. They are indicated at pin ERRN during Pwon/Listen-Only mode. No other measure is taken in the case of Bus Dominant Clamping.

10.1 Recovery from local failures

Whenever the pin RXD becomes dominant while TXD is recessive, the Local Failure flag is reset along with enabling the transmitter again. This indicates that a local failure like TXD Dominant Clamping, TXD/RXD Short Circuit or RXD Recessive Clamping does not exist. In Pwon/Listen-Only mode failure recovery is immediately reflected on the pin ERRN going HIGH again.

Another way to reset the Local Failure flag and to enable the transmitter is forcing a transition into Normal mode from any other mode. This reset option is necessary when there is no bus traffic i.e. the pin RXD does not become dominant. In this case the application microcontroller can force a transition to Normal mode after it has read the error status in Pwon/Listen-Only mode. If the failure is still present, it is detected again, disabling the transmitter. Alternatively, if the failure is cleared, normal operation is resumed. A suggested flow diagram for handling communication failures is shown in [Figure 16](#).

10.2 TXD dominant clamping

This fail-safe feature is already known from the TJA1050 and described in the Application Note AN00020 [Ref. 10](#). It prevents an erroneous CAN-controller from clamping the bus to dominant level by a continuously dominant TXD signal.

After a maximum allowable TXD dominant time $t_{DOM(TXD)}$ [Ref. 1](#) the transmitter is disabled. According to the CAN protocol [Ref. 2](#) only a maximum of eleven successive dominant bits are allowed on TXD (worst case of five successive dominant bits followed immediately by an error frame). Along with the minimum allowable TXD dominant time, this limits the minimum bit rate to 40 kbit/s.

10.3 TXD/RXD short circuit

Without the protection feature of the TJA1041(A), a TXD/RXD short circuit would result in a dead-lock situation clamping the bus dominant. If for example the transceiver receives a dominant signal, RXD outputs a dominant level. Because of the short circuit, TXD reflects a dominant signal, retaining the dominant bus state. As a result TXD and the bus are clamped continuously dominant. The resulting effect is the same as for the continuously

clamped dominant TXD signal. The TXD dominant timeout interrupts the deadlock situation by disabling the transmitter. The bus and also TXD become recessive again. However, the failure scenario may still exist and with the next dominant signal on the bus the described procedure will start again. Apparently, the TXD dominant timeout alone is not sufficient to protect the bus from a local TXD/RXD short circuit.

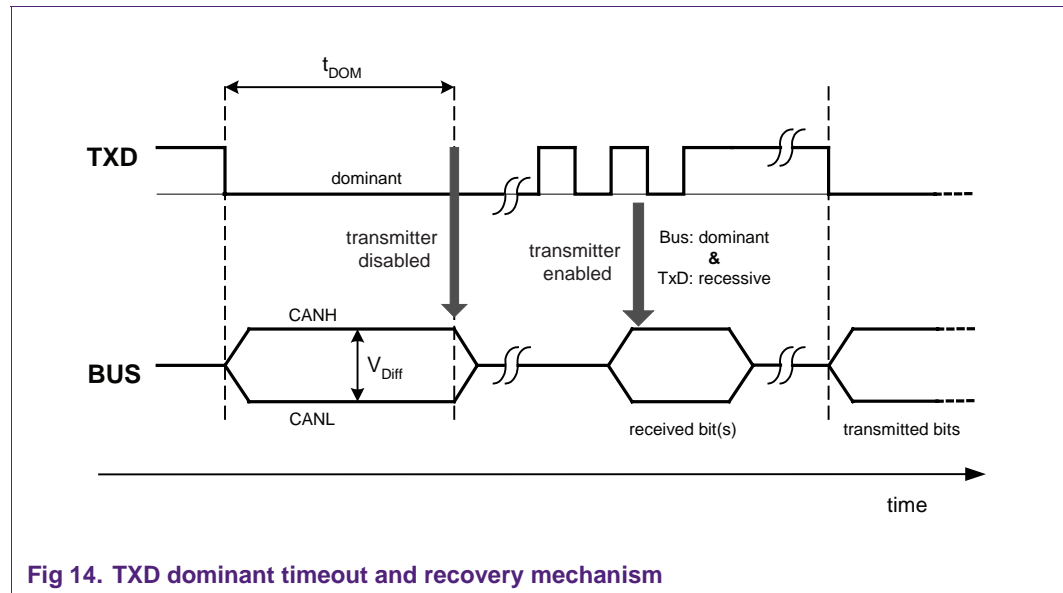


Fig 14. TXD dominant timeout and recovery mechanism

The TJA1041(A) keeps the transmitter off after detection of a TXD dominant clamping even if TXD gets released again. Failure recovery is performed first if the transceiver has detected a dominant bus signal while TXD is recessive. This is a clear indication that the TXD/RXD has short-circuited. Figure 14 illustrates the disabling and enabling of the transmitter with respect to a TXD/RXD short circuit. This way a local TXD/RXD short circuit will not disturb the communication of the remaining bus system.

10.4 RXD recessive clamping

If the pin RXD is shorted to V_{CC} or V_{IO} , the pin RXD is clamped to recessive signal. Using a conventional transceiver such a node assumes that the bus is permanently in Idle State. So it launches a message transmission on the bus whenever necessary, regardless of other bus traffic. As a result the bus traffic is heavily disturbed.

The TJA1041(A) can detect a RXD Recessive Clamping situation whenever it receives a dominant bus signal. On detection the transmitter is disabled immediately, so that the corrupted, non-synchronized node is prevented from disturbing the remaining bus traffic. The corrupted node is then excluded from communication. It can neither transmit nor receive any message, whereas the remaining bus is unaffected.

10.5 Bus dominant clamping

In the case of a short circuit from CANH to BAT/ V_{CC} , the circuit for the Common mode Stabilization may produce a differential voltage on the bus between CANH and CANL even if there is no dominant transmitting node. This is illustrated in Figure 15. The differential voltage can be high enough to represent a dominant signal ($V_{diff} > 0,9 V$). The result may be a permanently dominant clamped bus in the case of a short circuit from CANH to BAT.

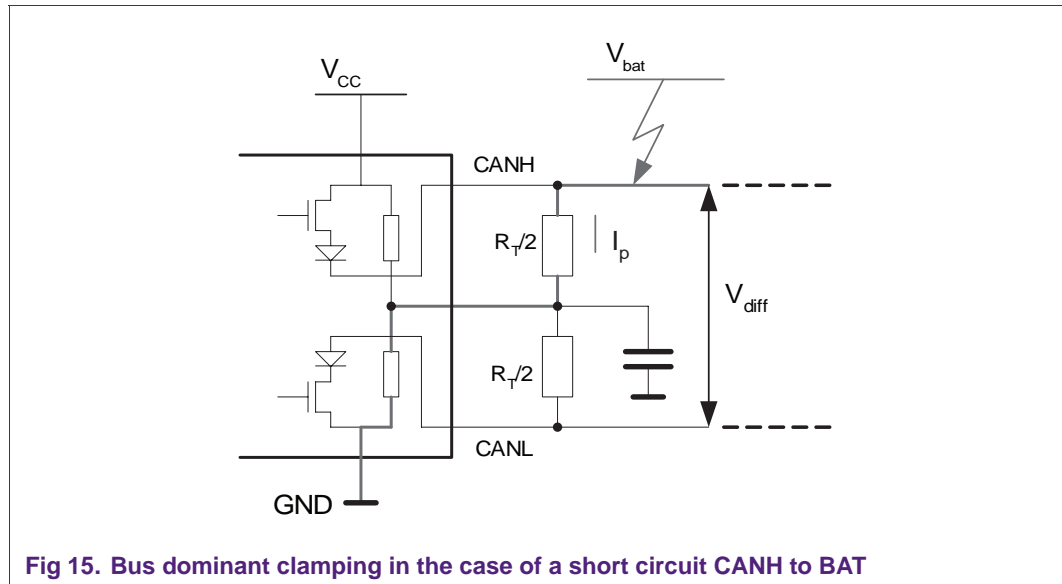


Fig 15. Bus dominant clamping in the case of a short circuit CANH to BAT

The TJA1041(A) can detect and report a Bus Dominant Clamping situation. If the receiver detects a bus dominant phase of longer than the bus dominant time out $t_{DOM(bus)}$ [Ref. 1](#) , this is indicated at pin ERRN in Pwon/Listen-Only mode.

10.6 Over temperature protection

An over-temperature condition may occur either if the transceiver is operated in an environment with high ambient temperature or if there is a short circuit condition on the bus. To protect the transceiver from self-destruction the transmitter is disabled automatically whenever the junction temperature exceeds the allowed limit [Ref. 1](#). In addition the Local Failure flag is set, which can be read at pin ERRN in Pwon/Listen-Only mode.

After an over-temperature condition the transmitter of the TJA1041(A) is released if the junction temperature is below the limit and if there is a transition into Normal mode or reception of a dominant bus signal while TXD is recessive.

11. Under-voltage detection

Table 3. Supply undervoltage detection

Under-voltage on	Detection condition	Mode change to
V_{CC}	$V_{CC} < V_{CC(sleep)}$ for longer than under-voltage detection time [1]	Sleep
V_{IO}	$V_{IO} < V_{IO(SLEEP)}$ for longer than under-voltage detection time [1]	Sleep
V_{BAT}	$V_{BAT} < V_{BAT(stb)}$; no timeout	Standby

11.1 V_{CC}/V_{IO} under-voltage detection

On detection of a V_{CC} or V_{IO} under-voltage condition the transceiver is forced autonomously into Sleep mode overruling the current signal combination on pin STBN and pin EN. As a result, pin INH becomes floating, disabling the voltage regulator(s).

An under-voltage condition may occur if pin V_{CC} and/or pin V_{IO} are disconnected or if there is a short circuit from V_{CC} or V_{IO} to GND e.g. due to a broken capacitor. In the case of a short circuit, disabling the voltage regulator prevents flow of high short-circuit current.

The under-voltage condition must hold at least the “undervoltage detection time on V_{CC} and V_{IO} ” before the transceiver is forced into Sleep mode. This time-out is needed to suppress the under-voltage detection during ramping up of V_{CC}/V_{IO} , e.g. on wakeup from Sleep mode. A wakeup event either received from the bus or the pin WAKE wakes up the transceiver (INH switched on) along with trying to ramp up V_{CC} and/or V_{IO} again. If there is still an under-voltage condition on V_{CC} and/or V_{IO} , the transceiver is forced into Sleep mode again.

Notice there is no dedicated signal to inform the microcontroller about a V_{CC} under-voltage condition at the transceiver. However, the microcontroller can learn from a transceiver under-voltage condition by evaluating the pin INH. Whenever a V_{CC} or V_{IO} under-voltage has been detected by the transceiver, a pull-down resistor would pull the pin INH to LOW level.

11.2 V_{BAT} under-voltage detection

The TJA1041(A) monitors the battery supply voltage at the pin V_{BAT} . If the battery supply voltage falls below the BAT-under-voltage threshold [Ref. 1](#), the transceiver enters autonomously the Standby mode, overruling the mode control pins STBN and EN. An under-voltage condition on the pin V_{BAT} may occur for example, if the pin V_{BAT} has been disconnected, or temporarily during start of the engine (pulse 4 of ISO7637). The BAT-under-voltage threshold is related to the V_{CC} supply voltage. A BAT-under-voltage condition is detected only if $V_{BAT} < V_{CC} - 1.4$ V(typ.) and will be taken off again when V_{BAT} crosses the detection threshold $V_{BAT(STANDBY)}$ upwards, leaving mode control to pin STBN and EN.

In addition, whenever V_{BAT} falls below $V_{BAT(Pwon)}$ [Ref. 1](#), the PWON flag is set. The microcontroller has access to this flag via the pin ERRN when the Pwon/Listen-Only mode is entered from Sleep, Standby or Go-to-Sleep Command mode. A transition into Normal mode deletes the PWON flag. In this way the application microcontroller can know from a temporary, local battery under-voltage condition.

12. Pin FMEA

This chapter provides an FMEA (Failure Mode and Effect Analysis) for typical failure situations, when dedicated pins of the TJA1041(A) are short-circuited to supply voltages like V_{BAT} , V_{CC} , GND or to neighbored pins or simply left open. The individual failures are classified, due to their corresponding effects on the transceiver and bus communication in [Table 4](#).

Table 4. Classification of failure effects

Class	Effects
A	- Damage to transceiver - Bus may be affected
B	- No damage to transceiver - No bus communication possible
C	- No damage to transceiver - Bus communication possible - Corrupted node excluded from communication
D	- No damage to transceiver - Bus communication possible - Reduced functionality of transceiver

Table 5. FMEA matrix for pin short-circuits to V_{BAT} and V_{CC}

Pin	Short to V_{BAT} (12 V ... 40 V)		Short to V_{CC} (5 V)	
	Class	Remarks	Class	Remarks
(1) TXD	A	Limiting value exceeded	C	TXD clamped recessive
(2) GND	C	Node is left unpowered	C	V_{CC} under-voltage detected; TRX goes to Sleep
(3) V_{CC}	A	Limiting value exceeded	---	---
(4) RXD	A	Limiting value exceeded	C	RXD recessive clamping, transmitter disabled
(5) V_{IO}	A	Limiting value exceeded	C	μC may be damaged if $V_{CC} > V_{IO}$
(6) EN	A	Limiting value exceeded	D	Standby and Pwon/Listen-Only not selectable
(7) INH	D	Voltage regulator keeps permanently	D	Voltage regulator keeps permanently on
(8) ERRN	A	Limiting value exceeded	D	No failure signaling to μC
(9) WAKE	D	Local wakeup not possible	D	Local wakeup not possible
(10) V_{BAT}	---	---	A	Limiting value exceeded
(11) SPLIT	D	Bus charged to BAT-level; bit timing problems possible	D	Bus charged to V_{CC} level; bit timing problems possible

Table 5. FMEA matrix for pin short-circuits to V_{BAT} and V_{CC} ...continued

Pin	Short to V_{BAT} (12 V ... 40 V)		Short to V_{CC} (5 V)	
	Class	Remarks	Class	Remarks
(12) CANL	B	No bus communication	B	No bus communication
(13) CANH	D	Degradation of EMC; bit timing problem possible	D	Degradation of EMC; bit timing problem possible
(14) STBN	A	Limiting value exceeded	D	Standby and Goto-Sleep not selectable

Table 6. FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open	
	Class	Remarks	Class	Remarks
(1) TXD	C	TXD dominant clamping; transmitter disabled	C	TXD clamped recessive
(2) GND	---	---	C	Under-voltage detected; TRX goes to Sleep
(3) V_{CC}	C	V_{CC} Under-voltage detected; TRX goes to Sleep	C	V_{CC} Under-voltage detected; TRX goes to Sleep
(4) RXD	C	RXD clamped dominant	C	μC likely to go into Bus-Off
(5) V_{IO}	C	V_{IO} Under-voltage detected; TRX goes to Sleep	C	V_{IO} under-voltage detected; TRX goes to Sleep
(6) EN	C	Normal and Goto-Sleep not selectable	C	Normal and Goto-Sleep not selectable
(7) INH	C	Voltage regulator keeps permanently off	C	Voltage regulator switched off
(8) ERRN	D	No failure signaling to μC	D	No failure signaling to μC
(9) WAKE	D	Local wakeup not possible	D	Local wakeup not possible
(10) V_{BAT}	C	Node is left unpowered	C	V_{BAT} under-voltage detected, TRX goes to Standby
(11) SPLIT	D	Bus discharged to GND-level; bit timing problems possible	D	No DC common mode stabilization
(12) CANL	D	Degradation of EMC, bit timing problem possible	C	Transmitting not possible
(13) CANH	B	No bus communication	C	Transmitting not possible
(14) STBN	C	Normal and Pwon/Listen-Only not selectable	C	Normal and Pwon/Listen-Only not selectable

Table 7. FMEA matrix for pin short-circuits between neighbored pins

Pin	Short to neighbored pin	
	Class	Remark
TXD-GND	C	Transmitter disabled after TXD Dominant Timeout
GND- V_{CC}	C	V_{CC} under-voltage detected; transceiver goes to Sleep
V_{CC} -RXD	C	RXD recessive clamping; transmitter disabled
RXD- V_{IO}	C	RXD recessive clamping; transmitter disabled

Table 7. FMEA matrix for pin short-circuits between neighbored pins ...continued

Pin	Short to neighbored pin	
	Class	Remark
V _{IO} -EN	D	Standby and Pwon/Listen-Only not selectable
EN-INH	D	Voltage regulator may switch off in Standby and Pwon/Listen-Only
ERRN-WAKE	D	Local wakeup not possible, damage to transceiver only with closed high-side switch
WAKE-V _{BAT}	D	Local wakeup not possible
V _{BAT} -SPLIT	D	Bus charged to BAT-level
SPLIT-CANL	D	Degradation of EMC
CANL-CANH	B	No bus communication
CANH-STBN	D	Transceiver is not able to enter low-power mode if the bus is driven dominant

13. Software issues

13.1 Software flow for handling communication failures

[Figure 16](#) suggests a software flow for handling communication failures. Starting from normal operation with the TJA1041(A) in Normal mode, the host microcontroller reads the Bus Failure flag at the pin ERRN whenever a communication failure has been reported by an error interrupt of the CAN-controller or by a missing transmit interrupt.

If the Bus Failure flag is set, the communication failure is likely to be caused by a bus failure. After a defined time-out period a new transmission attempt is performed. After a maximum number of transmission attempts have failed, an application appropriate fall-back procedure must be activated. On the other hand, if the Bus Failure flag is not set, the communication failure is likely to be caused by a local failure. In order to check for a local failure condition, the transceiver is forced into Pwon/Listen-Only mode. If a local failure is signalled (see [Section 10](#)), the application waits for recovery reading periodically the Local Failure flag. If there was no recovery within a defined time-out period, one option can be forcing a transition into Normal mode with releasing the transmitter. If the failure still exists, detection will disable the transmitter due to fail-safe reasons.

Another option is to use a fall-back procedure. If reading the Local Failure flag signals that the failure is recovered, the transceiver is put into Normal mode and normal operation continues.

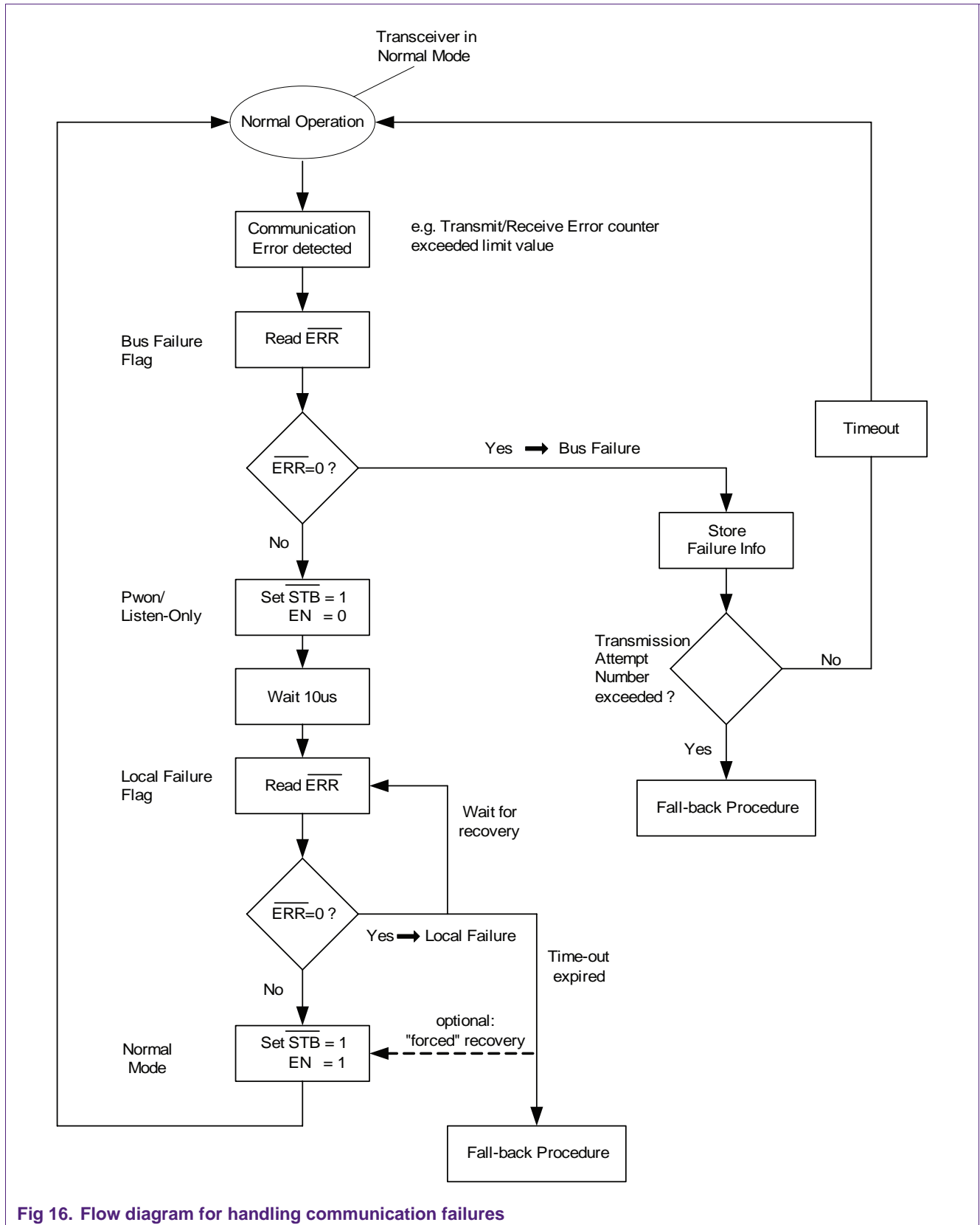


Fig 16. Flow diagram for handling communication failures

13.2 Software flow for an ECU cold start

The PWON flag of the TJA1041(A) indicates to the microcontroller whether a microcontroller cold start was caused by a wakeup from Sleep mode or by a first battery power application. This information is often needed for the application to initiate some possible calibration procedures on first battery power application.

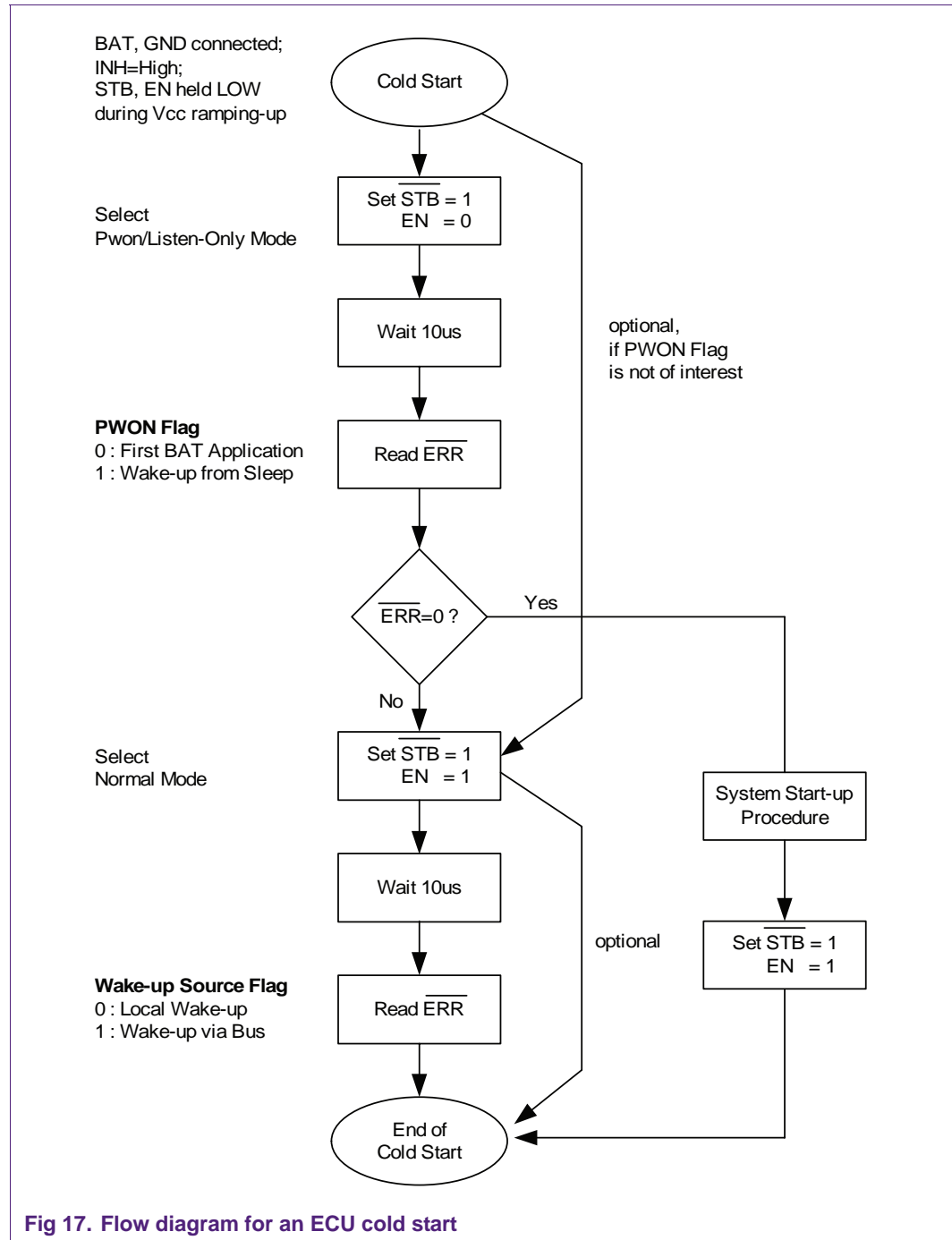


Fig 17. Flow diagram for an ECU cold start

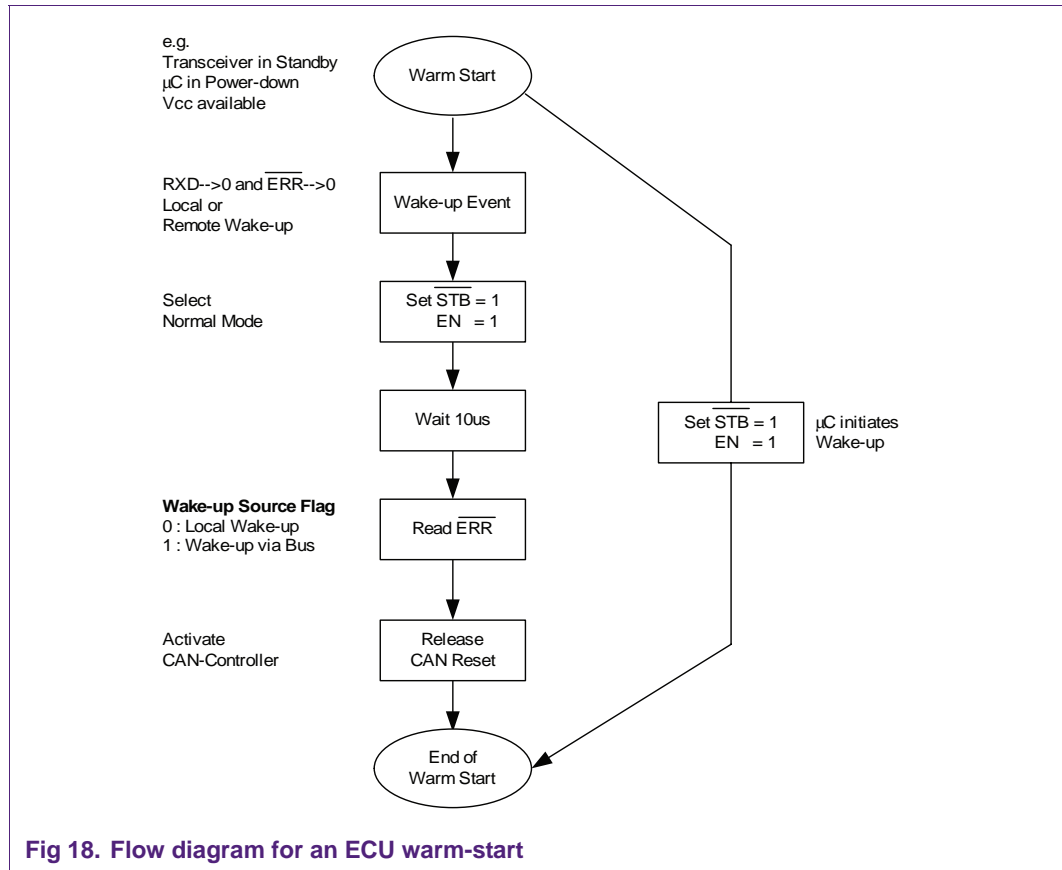
The pin ERRN reflects the PWON flag when entering the Pwon/Listen-Only mode from Standby, Sleep or Go-to-Sleep Command mode. Moreover, with a wakeup from Sleep mode the TJA1041(A) provides information on the wakeup source. Entering the Normal mode the pin ERRN reflects the Wakeup Source flag. A LOW signal indicates a local wakeup via the pin WAKE, whereas a HIGH signal indicates a remote wakeup via the bus.

If battery power is applied for the first time, an internal hardware reset signal is given to the transceiver for initialization. Subsequently the PWON flag is set and the pin INH is pulled to V_{BAT} , activating the voltage regulator(s) and ramping up the V_{CC} supply. Along with V_{CC} the pins RXD and ERRN go to HIGH level. With ramping up V_{CC} the microcontroller comes up. As almost all microcontrollers feature a weak pull-down or floating behavior at their port pins, the TJA1041 comes up in Standby mode after first battery power application. This is the starting point for the application program taking over the control now. If the microcontroller comes up with a HIGH level at its port pins, the TJA1041(A) enters immediately the Normal mode and the PWON flag information is irretrievably lost. [Figure 17](#) suggests a software flow for an ECU cold start. It considers primarily the issues related to the TJA1041(A) rather than representing a complete software flow. After the transceiver and microcontroller have performed their initialization, the transceiver is put into Pwon/Listen-Only mode for reading the PWON flag. If a LOW signal is read on the pin ERRN, the ECU cold start was initiated by first battery power application and the microcontroller performs the corresponding system start-up procedure. If a HIGH signal is read, the cold start was initiated by a wakeup from Sleep mode. In order to get information on the wakeup source, Normal mode is selected. If reading pin ERRN yields a LOW signal, there was a local wakeup via the pin WAKE. If reading yields a HIGH signal, the wakeup came via the bus. Afterwards, the cold start procedure ends and normal operation continues.

13.3 Software flow for an ECU warm start

A warm start is performed when the ECU wakes up from Standby (low power level 1). [Figure 18](#) suggests a software flow for an ECU warm-start. The starting point assumes a TJA1041 transceiver in its Standby mode and the host microcontroller in a dedicated power-down mode if available. If the transceiver receives a wakeup either via the bus or via the pin WAKE, the internal wakeup flag is set and signalled at the pin ERRN and RXD. These signals can be used for wakeup of the microcontroller from its power-down mode. The starting application program can now take control over the transceiver. If the PWON flag is of interest, the microcontroller can force the transceiver into Pwon/Listen-Only mode for reading the PWON flag. Otherwise the microcontroller can force the transceiver directly into Normal mode for reading the Wakeup Source flag at the pin ERRN.

As the microcontroller remains powered by the V_{CC} supply, the microcontroller can monitor its port pins for possible wakeup events. On detection of a wakeup event the microcontroller can initiate a wakeup by forcing the transceiver directly into Normal mode. Then reading of the PWON flag or Wakeup Source flag is not necessary.



13.4 How to enter Standby mode (low power level 1)

When the network management decides to put the bus system into Standby, each ECU must receive an appropriate standby command. The flow diagram in [Figure 19](#) shows the different steps in order to put the TJA1041(A) into Standby mode.

On receiving a standby command (e.g. using a certain CAN message) the microcontroller has to stop all CAN transmission. In order to ensure that no CAN communication is present on the bus, caused by other nodes, the bus must have been recessive for a suitable time before the TJA1041(A) is put into Standby mode by selecting STBN to LOW and EN to LOW level. If there is no system dependent “waiting period” implemented there would be the risk that a node sends out a last message while another one is already on the way towards Standby mode. This would cause a wakeup event making it impossible to enter a system wide low-power state.

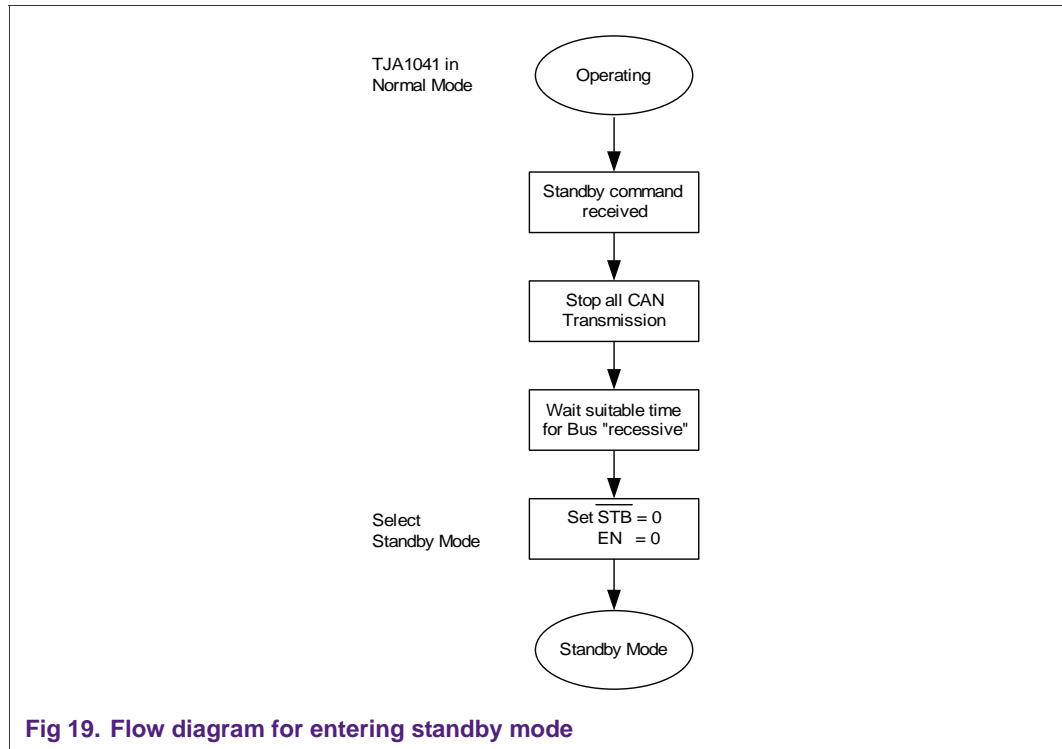
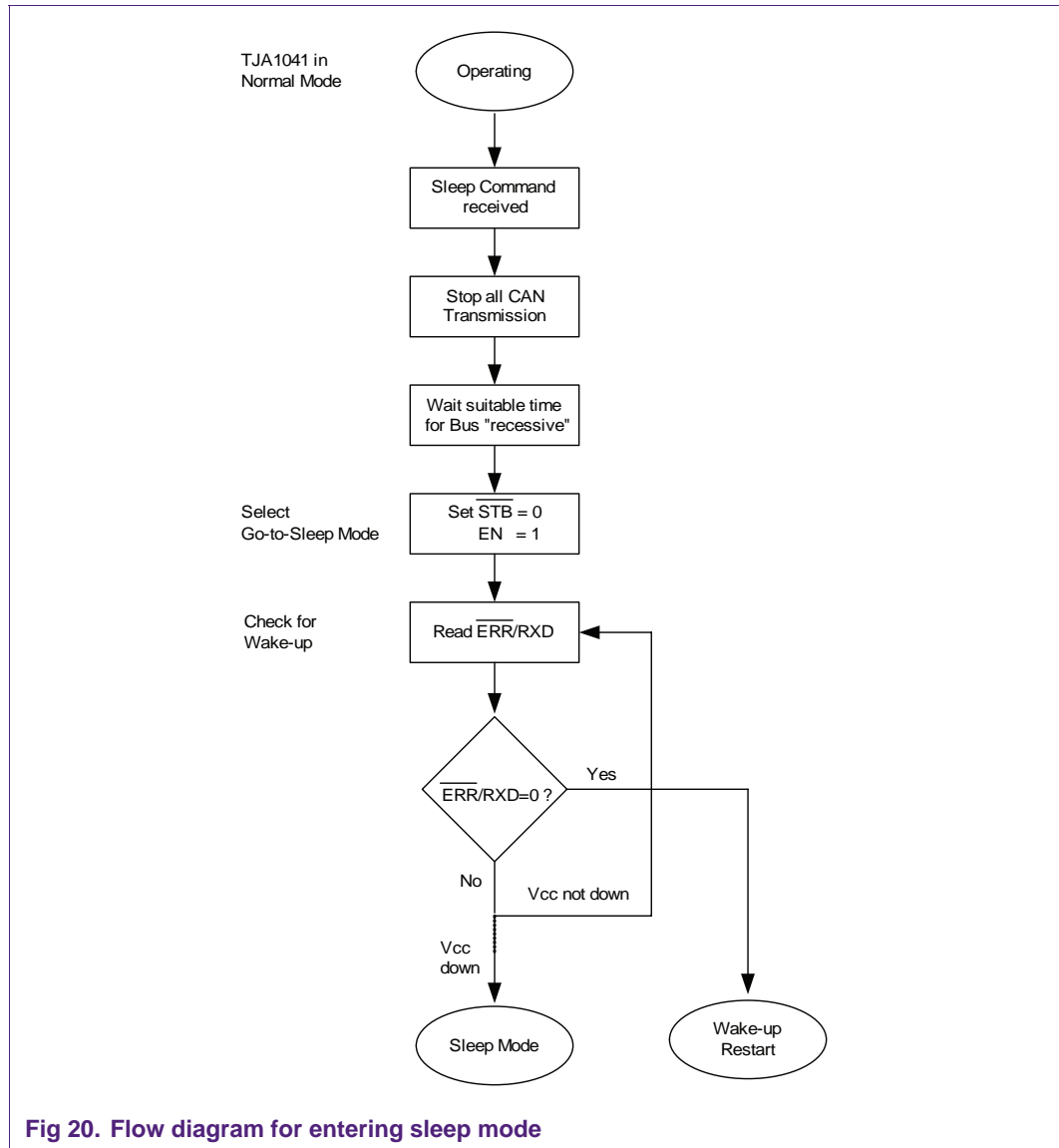


Fig 19. Flow diagram for entering standby mode

13.5 How to enter sleep mode (low power level 2)

The procedure to put an ECU into Sleep as shown in [Figure 20](#) is similar to the previous one for entering the Standby mode. On receiving a sleep command the microcontroller has to stop all CAN transmission. To ensure that no CAN communication is present on the bus, it must have been recessive for a suitable time before the TJA1041(A) is put into Sleep mode by selecting STBN to LOW and EN to HIGH level. The difference now is that the microcontroller checks periodically for a wakeup as long as V_{CC} is not yet down. This is necessary since it might happen that a wakeup event just appears while the Go-to Sleep Command is processed. In this case the INH of the TJA1041(A) remains HIGH and the V_{CC} does not drop. Instead, the wakeup request is forwarded to the application via RXD and ERR. Without this check the microcontroller would assume that a sleep phase follows with disabled V_{CC} , waiting forever for a power-on reset caused by a wakeup, which never happens.

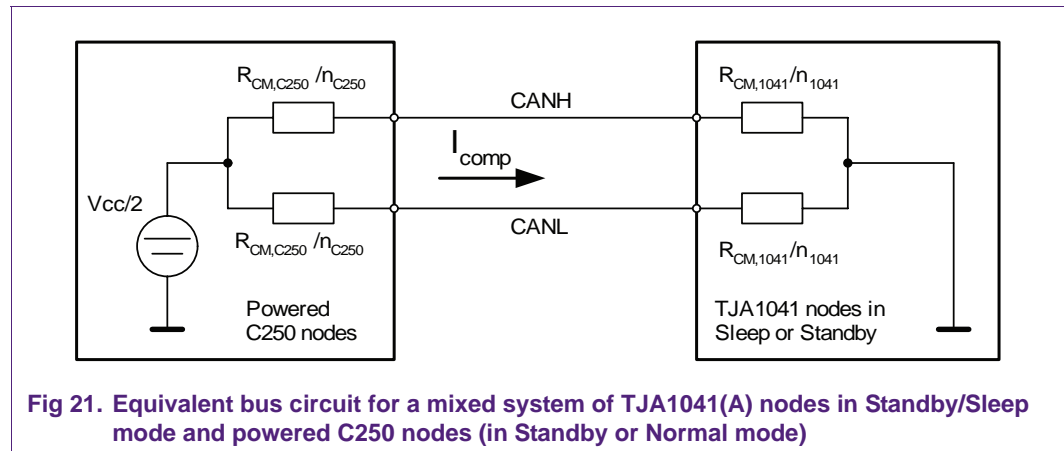


14. Interoperability

Besides the TJA1041(A), NXP Semiconductors offers the PCA82C250, PCA82C251, TJA1050 and TJA1040 high speed CAN transceiver products. Since all products are compatible with the ISO11898 standard, interoperability with each other is in principle guaranteed. They are able to work together in the same bus network. There are some issues related to different bus biasing behavior during low-power operation, which shall be considered in this chapter. [Table 8](#) shows the bus biasing in the different operation modes as well as in un-powered condition. Whenever there is a difference in the bus biasing, a steady DC common mode current will flow within the system. The common mode input resistance mainly defines the amount of this common mode current. This is shown in [Figure 21](#) for a bus in recessive state including TJA1041(A) and C250 nodes.

Table 8. Bus biasing of NXP transceivers depending on operation mode

Transceiver	Operation mode	Bus bias
TJA1041	Normal, Pwon/Listen-Only	$V_{CC}/2$
	Standby, Sleep, Go-to-Sleep, Un-powered	weak GND
TJA1040	Normal	$V_{CC}/2$
	Standby	weak GND
	Un-powered	Floating
TJA1050	Normal, Silent	$V_{CC}/2$
	Un-powered	weak GND
C250/C251	Normal, Standby	$V_{CC}/2$
	Un-powered	GND



Due to the big common mode input resistance CAN communication is not affected while parts of the network are still in low-power mode, while other nodes have already started communication. However, degradation of the emission performance is expected.

The following formula calculates the DC common mode current in a mixed system of TJA1041(A) and C250 nodes.

$$I_{comp,max} = \frac{V_{CC}/2}{R_{CM(C250)}/(2n_{C250}) + R_{CM(TJA1041)}/(2n_{TJA1041})} \tag{3}$$

with:

n_{C250} : number of nodes powered C250

$n_{TJA1041}$: number of nodes of TJA1041 in Standby/Sleep mode

$R_{CM(C250)}$ = 5k min common mode input resistance of C250 at pin CANH/L

$R_{CM(TJA1041)}$ = 15k min common mode input resistance of TJA1041 at pin CANH/L

Table 9. Conditions leading to DC common mode current

Transceiver		TJA1041				
		Normal	PWON/Listen only	Standby	Sleep	Go to sleep
TJA1040	Normal	---	---	X	X	X
	Standby	X	X	---	---	---
	Un-powered	---	---	---	---	---
TJA1050	Normal	---	---	X	X	X
	Silent	---	---	X	X	X
	Un-powered	X	X	---	---	---
C250/C251	Normal	---	---	X	X	X
	Standby	---	---	X	X	X
	Un-powered	X	X	---	---	---

X : DC common mode current --- : no DC common mode current

14.1 TJA1041(A) mixed with C250/C251/TJA1050 nodes

[Table 9](#) identifies the conditions leading to different bus biasing and DC common mode current. There is some compensation current in case TJA1041(A) nodes are in Normal (High speed) mode, while other C250/C251/TJA1050 nodes are left un-powered. Moreover, common mode current occurs when TJA1041(A) nodes are in Standby/Sleep/Go-to-Sleep mode, while other C250/C251/TJA1050 nodes are kept powered in any operation mode. However, the common mode current is negligible.

14.2 TJA1041(A) mixed with TJA1040 nodes

[Table 9](#) reveals also that in a mixed system of TJA1040 and TJA1041(A) nodes, it is not expected to have situations of different bus biasing. In the low-power modes both the TJA1040 and TJA1041(A) show a weak termination to GND. When the bus is in power-down with all nodes either in Standby or Sleep mode, there will be no DC common mode current. During normal CAN operation, when all nodes are into Normal (High speed) or Pwon/Listen-Only mode for diagnosis features, the bus is collectively biased to $V_{CC}/2$. There will be no DC common mode current.

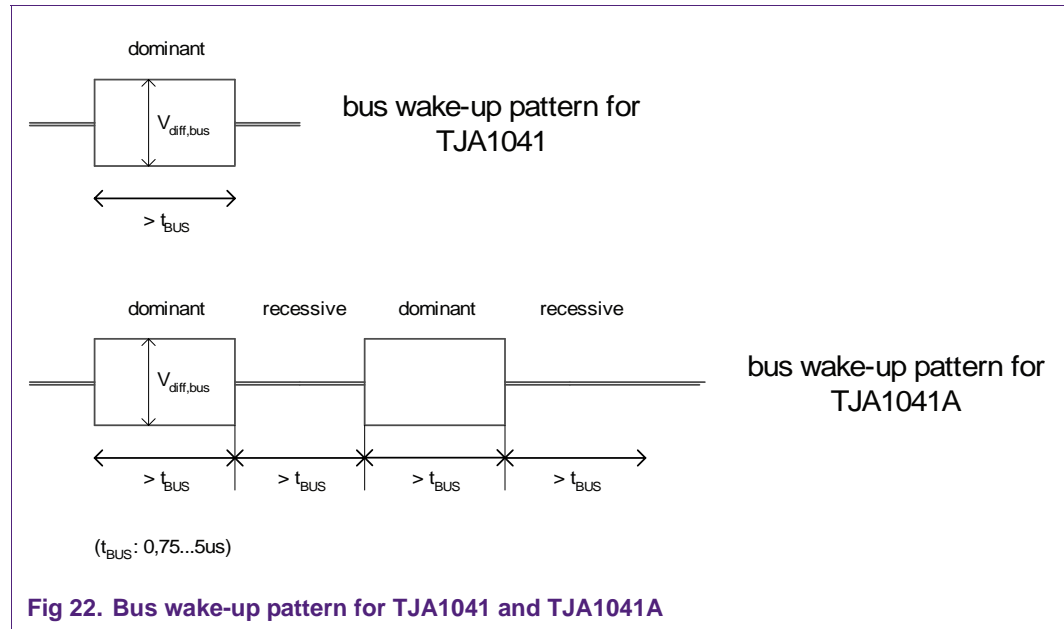
15. Appendix

15.1 Differences between TJA1041 and TJA1041(A)

The only difference between the TJA1041 and TJA1041A concerns the bus wakeup mechanism. The TJA1041 detects a bus wake-up request when the bus remains in dominant state for at least 5 μ s. In contrast to that, the TJA1041A detects a bus wake-up request when the bus shows two dominant phases of at least 5 μ s duration, with each dominant phase followed by a recessive phase of at least 5 μ s. [Figure 22](#) illustrates the wake-up pattern requirements for the TJA1041 and TJA1041A.

The enhanced bus wakeup detection offers improved robustness against unwanted wakeup in presence of bus failures, especially for large networks. There will be no unwanted bus wake-up due to a BAT-to-CANH short-circuit or CANL wire interruption, while the system is entering Bus Sleep.

At a data rate of 500 kbit/s, a single arbitrary CAN data frame is not necessarily sufficient to launch a remote wake-up with the enhanced wake-up pattern. Here, two consecutive arbitrary CAN data frames are needed to reliably launch a remote wake-up. At 125 kbit/s data rate, any CAN data frame on the bus leads to a remote wake-up of the TJA1041A transceiver.



15.2 Maximum power dissipation within termination resistors

With the help of [Figure 23](#) the maximum power dissipation within the termination resistors in the case of a bus short circuit is calculated. Assuming a max. short-circuit voltage of 40 V on the bus, the max. short-circuit current, which may flow within the TJA1041 while transmitting dominant, is limited to 95 mA [Ref. 1](#). As shown in the figure, when one node is transmitting a dominant bit, this short-circuit current is distributed to the two bus terminations, so that each 60 Ω termination resistor would dissipate power of:

$$P_{dom} = 60 \Omega \times (95 \text{ mA} / 2)^2 = 135 \text{ mW}$$

The average power dissipation is reduced according to the average recessive/dominant duty cycle on TXD.

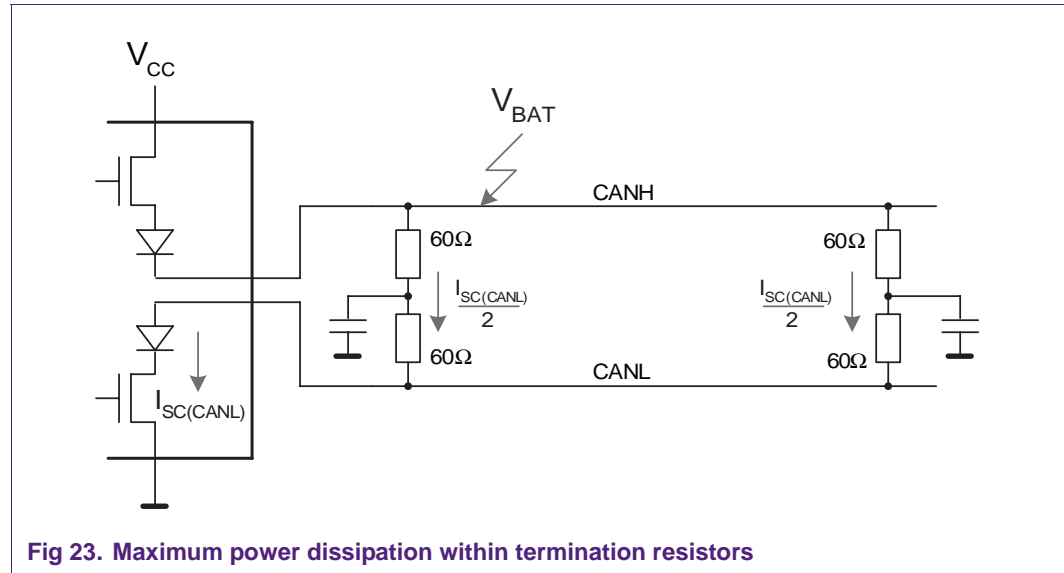


Fig 23. Maximum power dissipation within termination resistors

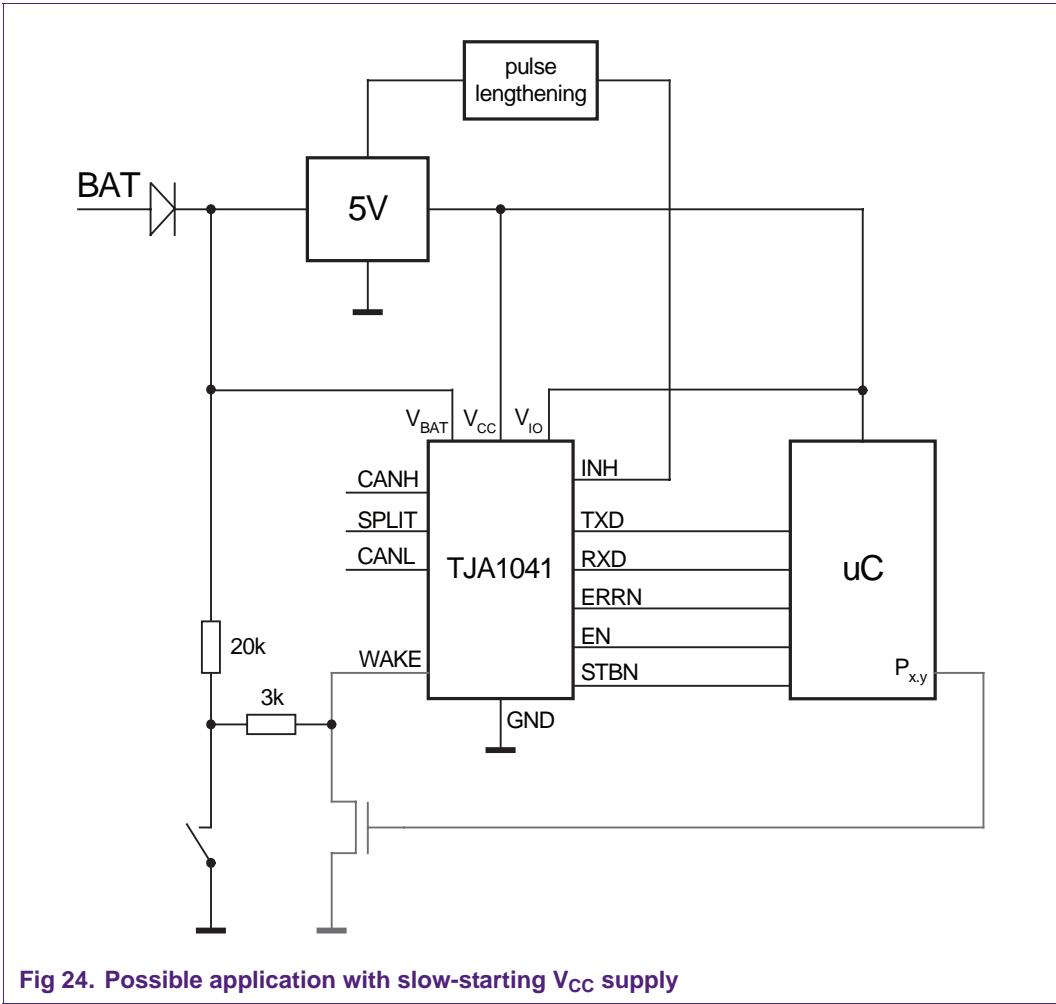
15.3 Application with slow-starting V_{CC} supply

For a successful start-up of the TJA1041(A) the V_{CC} and V_{IO} supply voltage has to ramp up within at least the min. “under-voltage detection time on V_{CC} or V_{IO}” [Ref. 1](#) after BAT power application or after a wakeup from Sleep mode (with disabled V_{CC} supply). If the INH controlled supply starts too slowly, the TJA1041(A) may detect a V_{CC}/V_{IO} under-voltage condition, forcing the transceiver into Sleep mode. These applications with slow starting supplies would need an extra local wakeup impulse via the pin WAKE to get the node alive. [Figure 24](#) sketches a possible solution, which can generate an extra local wakeup impulse. It includes measures to elongate the INH “On” signal and a transistor switch at the pin WAKE, such that a local wakeup pulse can be applied from the microcontroller.

As the wakeup circuit needs some time for recovery (“under-voltage recover time on V_{CC} and V_{IO}” [Ref. 1](#)) after a V_{CC}/V_{IO} under-voltage has been detected, the extra local wakeup pulse should be given to the transceiver earliest after the max. recovery time from point of the under-voltage detection. The diagram in [Figure 25](#) illustrates the timing in more detail.

After BAT power application to the TJA1041(A) the transceiver is initialized, activating INH almost immediately.

1. Because of the large delay in ramping up V_{CC}, the transceiver may detect a V_{CC}/V_{IO} under-voltage condition as early as 5 ms after battery power application, switching off the INH pull-up current and leaving the pin floating.
2. However, due to the INH pulse lengthening, the voltage regulator still keeps active, allowing complete ramp-up of V_{CC} and initializing the microcontroller.
3. As soon as the maximum under-voltage recovery time [Ref. 1](#) has expired, the microcontroller can generate a local wakeup to the transceiver. This wakeup should be applied first after V_{CC} has completely ramped up. As a result the transceiver wakes up from Sleep mode, entering the mode currently selected at the mode control pins STBN and EN.



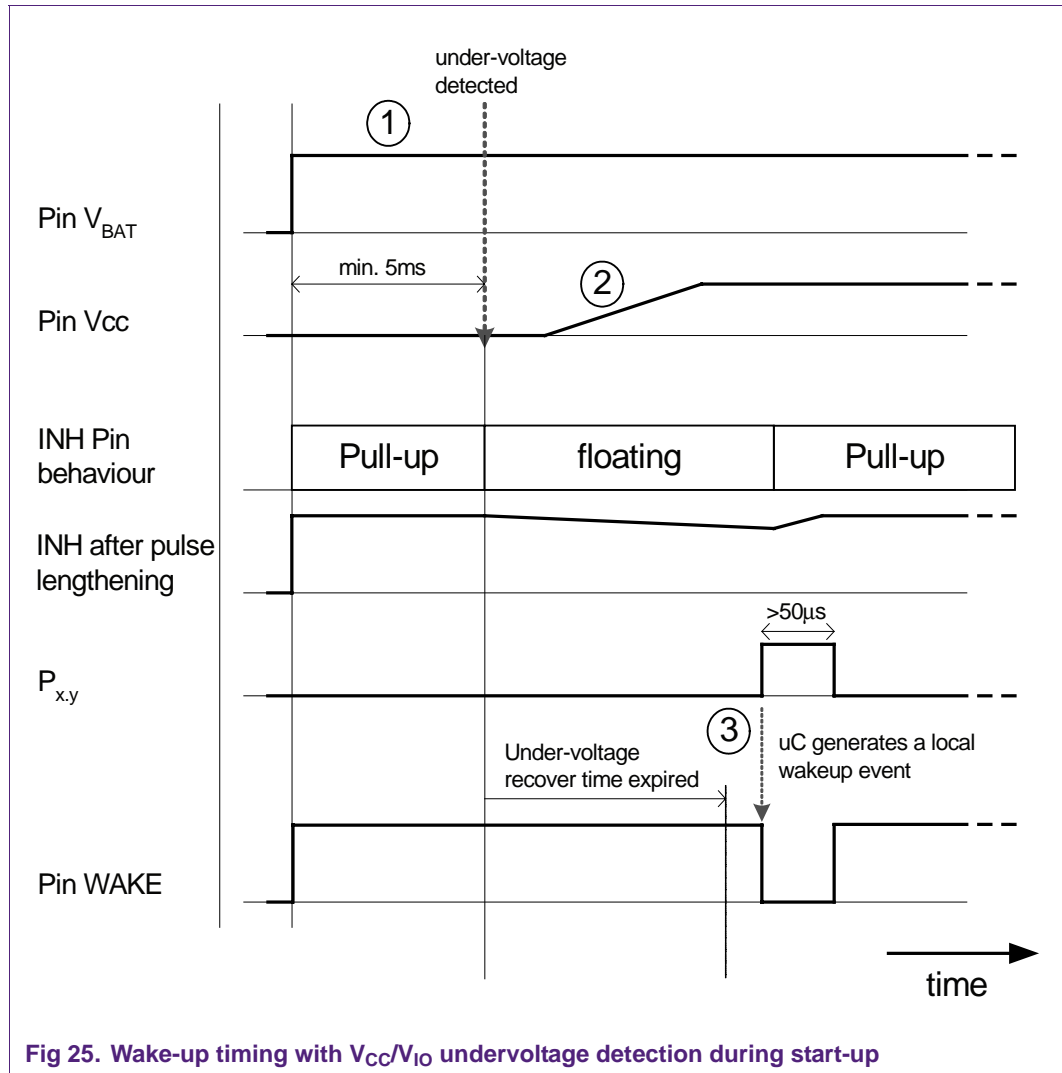


Fig 25. Wake-up timing with V_{CC}/V_{IO} undervoltage detection during start-up

15.4 V_{CC} supply

Typically a capacitor between 47-100 nF is recommended being connected between V_{CC} and GND close to the transceiver. This capacitor buffers the supply voltage during the transition from recessive to dominant, when there is a sharp rise in current demand. An additional bypass capacitor is usually placed at the output of the voltage regulator. Its purpose is to buffer disturbances on the battery line and to buffer extra supply current demand in the case of bus failures. The calculation of the bypass capacitor value is shown in [Section 15.4.2](#), while in [Section 15.4.1](#) the average V_{CC} supply current is calculated for thermal load considerations of the V_{CC} voltage regulator. This can be done in the absence and in the presence of bus short-circuit conditions.

15.4.1 Thermal load consideration for the V_{CC} voltage regulator

The average V_{CC} supply current can be calculated in absence and in presence of bus short-circuit conditions. The maximum average supply current in absence of bus failures calculates to:

$$I_{CC_norm_avg} = 0.5 \cdot (I_{CC_rec_max} + I_{CC_dom_max}) \tag{4}$$

Example:

With $I_{CC_rec_max} = 10$ mA and $I_{CC_dom_max} = 80$ mA [Ref. 1](#) this results in an average supply current of 45 mA. Here a transmit duty cycle of 50 % on pin TXD is assumed.

In presence of bus failures the V_{CC} supply current for the transceiver can increase significantly. The maximum dominant V_{CC} supply current $I_{CC_dom_sc_max}$ flows in the case of a short circuit from CANH to GND. Along with the CANH short circuit output current $I_{SC(CANH)}$ the maximum dominant V_{CC} supply current $I_{CC_dom_sc_max}$ calculates to about 120 mA. This results in an average supply current of 65 mA in worst case of a short circuit from CANH to GND. The V_{CC} voltage regulator must be able to handle this average supply current.

15.4.2 Dimensioning the bypass capacitor of the voltage regulator

Dimensioning the bypass capacitor gets very important with a shared voltage supply between transceiver and microcontroller. Here, extra current demand with bus failures may not lead to an unstable supply for the microcontroller. Following the extra current demand in the case of bus failures is calculated. This input is used to determine the bypass capacitor needed to keep the voltage supply stable under the assumption that all the extra current demand has to be delivered from the bypass capacitor.

The quiescent current delivered from the voltage regulator to the transceiver is determined by the recessive V_{CC} supply current I_{CC_rec} .

Extra supply current is demanded during dominant transmitting periods. It is calculated by:

$$\Delta I_{CC_ex} = I_{CC_dom} - I_{CC_rec} \quad (5)$$

In absence of bus failures the maximum extra supply current is calculated by:

$$\Delta I_{CC_max} = I_{CC_dom_max} - I_{CC_rec_min} \quad (6)$$

Example:

With $I_{CC_dom_max} = 80$ mA and $I_{CC_rec_min} = 2$ mA the maximum extra supply current calculates to 78 mA. Normally, the voltage regulator is strong enough to deliver this extra supply current without significant V_{CC} voltage drop.

In presence of bus failures the maximum extra supply current may be significantly higher. Considering the worst case of a short circuit from CANH to GND the maximum extra supply current is calculated by:

$$\Delta I_{CC_max_sc} = I_{CC_dom_sc_max} - I_{CC_rec_sc_min} \quad (7)$$

Example:

With $I_{CC_dom_sc_max} = 120$ mA (estimated) and $I_{CC_rec_sc_min} = 2$ mA the maximum extra supply current calculates to 118 mA.

In the case of a short circuit from CANH to GND, the bus is clamped to the recessive state, and according to the CAN protocol the CC transmits 17 subsequent dominant bits on TXD. That would mean the above calculated maximum extra supply current has to be delivered for at least 17 bit times. The reason for the 17 bit times is that at the moment the CAN controller starts a transmission, the dominant Start Of Frame bit is not fed back to

RXD and forces an error frame due to the bit failure condition. The first bit of the error frame again is not reflected at RXD and forces the next error frame (TX Error Counter +8). Latest after 17 bit times, depending on the TX Error Counter Level before starting this transmission, the CAN controller reaches the Error Passive limit (128) and stops sending dominant bits. Now a sequence of 25 recessive bits follows (8 Bit Error Delimiter + 3 Bit Intermission + 8 Bit Suspend Transmission) and the V_{CC} supply current becomes reduced to the recessive one.

Assuming that the complete extra supply current during the 17 bit times has to be buffered by the bypass capacitor, the worst-case bypass capacitor calculates to:

$$C_{Buff} = \frac{\Delta I_{CC_max_sc} \cdot t_{dom_max}}{\Delta V_{max}} = \frac{118 \text{ mA} \cdot 34 \mu s}{0.2 \text{ V}} \approx 20 \mu F \tag{8}$$

with:

$$\Delta I_{CC_max_sc} = 118 \text{ mA} \tag{9}$$

maximum extra supply current in the case of a short circuit from CANH to GND:

$$t_{dom_max} = 34 \mu s \tag{10}$$

dominant time of 17 bit times at 500 kbit/s:

$$\Delta V_{max} = 0.2 \text{ V} \tag{11}$$

maximum allowed V_{CC} voltage drop:

Of course, depending on the regulation capabilities of the used voltage regulator the bypass capacitor may be much smaller.

16. Abbreviations

Table 10. Abbreviations

Acronym	Description
CAN	Controller Area Network
Clamp-15	ECU architecture, Battery supply line after the ignition key, module is temporarily supplied by the battery only (when ignition key is on)
Clamp-30	ECU architecture, direct battery supply line before the ignition key, module is permanently supplied by the battery
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
EME	Electromagnetic Emission
EMI	Electromagnetic Immunity
FMEA	Failure Mode and Effects Analysis
SOI	Silicon On Insulator

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